TEXAS INSTRUMENTS

Linear Circuits

3-V Family

Data Book

1992

Linear Products

Linear Products Quick Reference Guide

Data Book	Contents	Document No.
• Optoelectronics and Image Sensors	Optocouplers CCD Image Sensors and Support Phototransistors IR-Emitting Diodes	SOYD002, 1990
• Speech System Manuals	TSP50C4X Family TSP50C10/11 Synthesizer TSP53C30 Synthesizer	SPSS010, 1990
• Interface Circuits	Data Transmission and Control Circuits, Peripheral Drivers/Power Actuators, Display Drivers	SLYD006, 1991
• Telecommunications Circuits	Transmission, Switching, Subscriber, Transient Suppressors	SCTD001B, 1991
• Linear and interface Circuits Applications	Op Amps/Comparators, Video Amps, VRegs, Power Supply Design, Timers Display Drivers, Datran, Peripheral Drivers, Data Acq., Special Functions	SLYA005, 1991
• Mass Storage ICs Designer's Reference Guide	Disk Drivers: Read/Write, Servo/System Control, Interface/Linear, Digital ASIC, LinASIC™, Applications	SSCA001, 1992
• Macromodel Data Manual	Level I: Operational Amplifiers, Voltage Comparators, Building Blocks Level II: Selected Operational Amplifiers, Building Blocks	SLOS047B, 1992
• LinASIC Library Summary	Mixed Signal Standard Cells	SLXS001, 1992
• Linear Circuits Vol 1 Operational Amplifiers	Operational Amplifiers	SLYD003A, 1992
• Linear Circuits Vol 2 Data Conversion, DSP Analog Interface, and Video Interface	ADCs, DACs, DSP Analog Interfaces and Conversion, Video Interface Palettes, Analog Switches, Filters, Data Manuals	SLYD004A, 1992
• Linear Circuits Vol 3 Voltage Regulators/ Supervisors, Comparators, Special Functions, and Building Blocks	Voltage Regulators, Voltage Supervisors, Building Blocks, Comparators, Video Amplifiers, Hall-Effect Devices, Timers and Current Mirrors, Magnetic Memory Controllers, Sound Generators, Frequency-to-Voltage Converters, Sonar Ranging Circuits and Modules	SLYD005A, 1992

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Printed in the U.K.

INTRODUCTION

Texas Instruments offers the industry's first dedicated family of linear ICs that are specifically designed, characterized, and tested for operation at 3.3 V of less. Prefixed with "TLV" to indicate low-voltage operation, this family of analog circuits includes seven operational amplifiers, two voltage comparators, and a low dropout (LDO) voltage regulator.

Built using Texas Instruments LinCMOS™ process, the new operational amplifiers and comparators are optimized to operate down to 2V and the CMOS input stage ensures high impedance. The operational amplifiers are available as singles, duals, and quads with three levels of ac performance. Likewise, the comparators are offered as duals and quads.

All of the 3-V devices are available in the new thin-scaled small-outline package (TSSOP) as well as in the standard small-outline and through-hole packages. The TSSOP surface mount package is just 1.1mm (max) thick and can be a real space saver in densely packed designs.

While this manual only offers information on the first 3-V analog devices available for TI, complete technical data for upcoming 3-V devices or any TI semiconductor product is available from your nearest TI Field Sales Office, local authorized TI distributor, or by writing directly to:

Texas Instruments Incorporated
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P.O. Box 809066
Dallas, Texas 75380-9066

We sincerely feel that the new 3-V Family Data Book will be a significant addition to your library of technical literature for Texas Instruments.

General Information	1
Data Sheets	2
Mechanical Data	3

voltage regulator

$T_A = 25°C$

DESCRIPTION	OUTPUT VOLTAGE (V)	OUTPUT CURRENT RATING	OUTPUT VOLTAGE TOLERANCE (±%)	TYPE	PACKAGE	PAGE NO.
Low-Dropout, 3.3 V Fixed	3.3	500 mA	1	TLV2217-33	KC, N, PW	2–3

operational amplifiers

$V_{DD} = 3$ V, $T_A = 25°C$

DESCRIPTION	SUPPLY VOLTAGE (V)		V_{IO} (mV)	I_{IB} (pA)	A_{VD} (V/mV)	B_1 (kHz)	SR (V/µs)	TYPE	PACKAGES	PAGE NO.
	MIN	MAX	MAX	TYP	MIN	TYP	TYP			
Dual, Low-Power	2	8	9	0.6	50	27	0.03	TLV2322I	D, P, PW	2–7
Quad, Low-Power	2	8	10	0.6	50	27	0.03	TLV2324I	D, N, PW	2–31
Dual, Medium-Power	2	8	9	0.6	25	300	0.43	TLV2332I	D, P, PW	2–55
Quad, Medium-Power	2	8	10	0.6	25	300	0.43	TLV2334I	D, N, PW	2–79
Single, Programmable High-Bias Mode Medium-Bias Mode Low-Bias Mode	 2 2 2	 8 8 8	 8 8 8	 0.6 0.6 0.6	 3 25 50	 790 300 27	 2.1 0.43 0.03	TLV2341I	D, P, PW	2–103
Dual, High-Speed	2	8	9	0.6	3	790	2.1	TLV2342I	D, P, PW	2–153
Quad, High-Speed	2	8	10	0.6	3	790	2.1	TLV2344I	D, N, PW	2–177

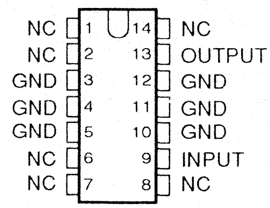
comparators

$V_{DD} = 3$ V, $T_A = 25°C$

DESCRIPTION	SUPPLY VOLTAGE MIN (V)	SUPPLY VOLTAGE MAX (V)	V_{IO} MAX (mV)	I_{IB} TYP (pA)	I_{OL} MIN (mA)	RESPONSE TIME TYP (ns)	TYPE	PACKAGES	PAGE NO.
Dual, Differential	2	8	5	5	6	200	TLV2352	D, P, PW	2–201
Quad, Differential	2	8	5	5	6	200	TLV2354	D, N, PW	2–213

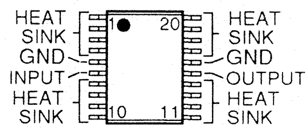
- Fixed 3.3-V Output
- ±1% Maximum Output Voltage Tolerance at T_J = 25°C
- 500-mV Maximum Dropout Voltage at 500 mA
- 500-mA Output Current
- ±2% Absolute Output Voltage Variation
- Internal Overcurrent Limiting
- Internal Thermal Overload Protection
- Internal Overvoltage Protection

N PACKAGE
(TOP VIEW)



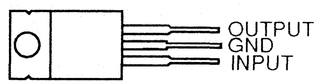
NC – No internal connection

PW PACKAGE
(TOP VIEW)



HEAT SINK – These pins have an internal resistive connection to ground and should be grounded.

KC PACKAGE
(TOP VIEW)



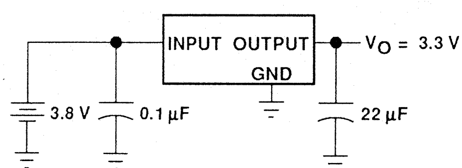
description

The TLV2217-33 is a low-dropout 3.3-V fixed voltage regulator. The regulator is capable of sourcing 500 mA of current with an input-output differential of 0.5 V or less. The TLV2217-33 provides internal overcurrent limiting, thermal overload protection, and overvoltage protection.

The 0.5-V dropout for the TLV2217-33 makes it ideal for battery applications in 3.3-V logic systems. For example, battery input voltage to the regulator may drop as low as 3.8 V, and the TLV2217-33 will continue to regulate the system. For higher voltage systems, the TLV2217-33 may be operated with a continuous input voltage of 12 V.

The TLV2217-33N and TLV2217-33KC cannot be harmed by temporary mirror image insertion. This regulator is characterized for operation from 0°C to 125°C virtual junction temperature.

typical application schematic



AVAILABLE OPTIONS

T_J	PACKAGE		
	PLASTIC POWER (KC)	PLASTIC DIP (N)	SURFACE MOUNT (PW)†
0°C to 125°C	TLV2217-33KC	TLV2217-33N	TLV2217-33PWLE

†The PW package is only available left-end taped and reeled.

TEXAS INSTRUMENTS

absolute maximum ratings over operating virtual junction temperature range (unless otherwise noted)

Continuous input voltage . . . . 16 V
Continuous total dissipation (see Note 1) . . . . See Dissipation Rating Table
Operating virtual junction temperature range . . . . –55°C to 150°C
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

NOTE 1: Refer to Figures 1 and 2 to avoid exceeding the design maximum virtual junction temperature; these ratings should not be exceeded. Due to variation in individual device electrical characteristics and thermal resistance, the built-in thermal overload protection may be activated at power levels slightly above or below the rated dissipation.

DISSIPATION RATING TABLE

PACKAGE	POWER RATING AT	T ≤ 25°C POWER RATING	DERATING FACTOR ABOVE T = 25°C	T = 70°C POWER RATING	T = 85°C POWER RATING	T = 125°C POWER RATING
KC	T_A	2000 mW	16 mW/°C	1280 mW	1040 mW	400 mW
	T_C†	20000 mW	182 mW/°C	14540 mW	11810 mW	4645 mW
N	T_A	2250 mW	18 mW/°C	1440 mW	1170 mW	450 mW
	T_C	11850 mW	94.8 mW/°C	7584 mW	6162 mW	2370 mW
PW	T_A	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
	T_C	4625 mW	37 mW/°C	2960 mW	2405 mW	925 mW

†Derate above 40°C

DISSIPATION DERATING CURVE
vs
FREE-AIR TEMPERATURE

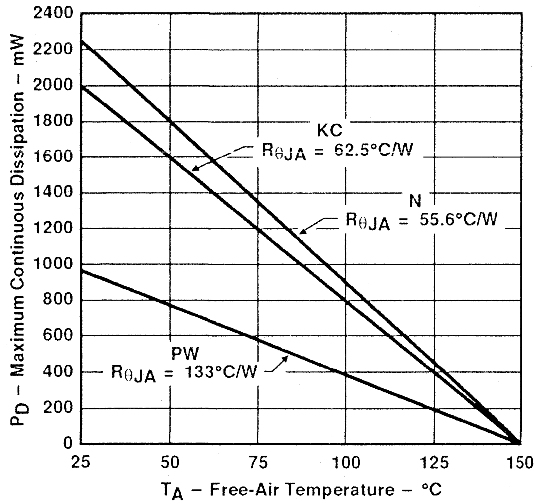


Figure 1

DISSIPATION DERATING CURVE
vs
CASE TEMPERATURE

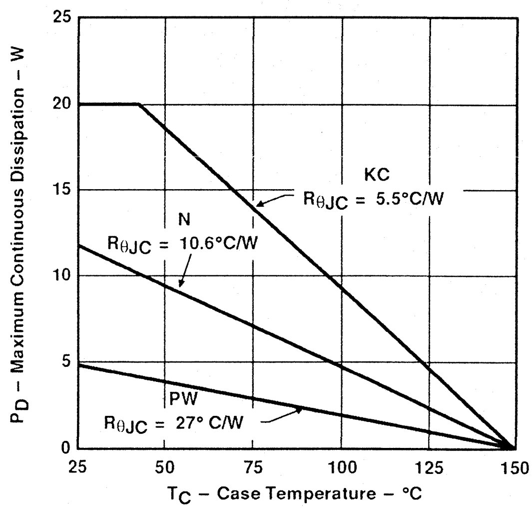


Figure 2

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, V_I	3.80	12.0	V
Output current, I_O	0	500	mA
Operating virtual junction temperature range, T_J	0	125	°C

electrical characteristics at V_I = 4.5 V, I_O = 500 mA, T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP	MAX	UNIT
Output voltage	I_O = 20 mA to 500 mA, V_I = 3.8 V to 5.5 V	T_J = 25°C	3.267	3.30	3.333	V
		T_J = 0°C to 125°C	3.234		3.366	
Input regulation	V_I = 3.8 V to 5.5 V			5	15	mV
Ripple rejection	f = 120 Hz, V_{ripple} = 1 V_{pp}			–62		dB
Output regulation	I_O = 20 mA to 500 mA			5	30	mV
Output noise voltage	f = 10 Hz to 100 kHz			500		μV
Dropout voltage	I_O = 250 mA				400	mV
	IO = 500 mA				500	
Bias current	I_O = 0			2	5	mA
	I_O = 500 mA			19	49	

† Pulse-testing techniques are used to maintain the virtual junction temperature as close to the ambient temperature as possible. Thermal effects must be taken into account separately. All characteristics are measured with a 0.1-μF capacitor across the input and a 22-μF tantalum capacitor with equivalent series resistance of 1.5 Ω on the output.

COMPENSATION CAPACITOR SELECTION INFORMATION

The TLV2217-33 is a low-dropout regulator. This means that the capacitance loading is important to the performance of the regulator because it is a vital part of the control loop. The capacitor value and the equivalent series resistance (ESR) both affect the control loop and must be defined for the load range and the temperature range. Figures 3 and 4 can be used to establish the capacitance value and ESR range for best regulator performance.

ESR OF OUTPUT CAPACITOR
vs
LOAD CURRENT

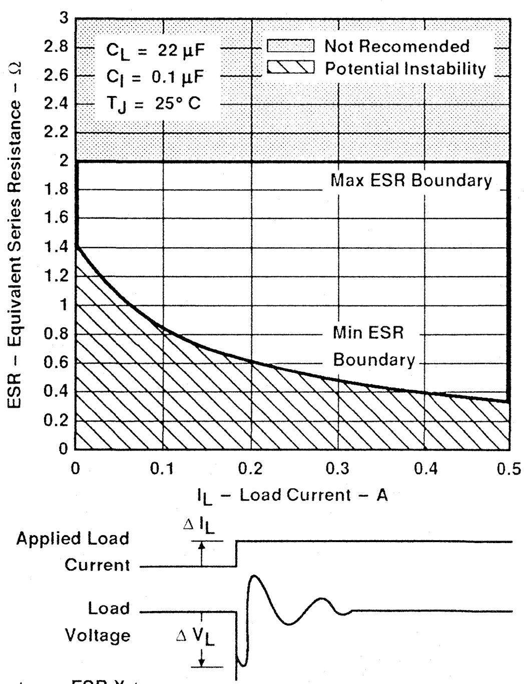


Figure 3

STABILITY
vs
ESR

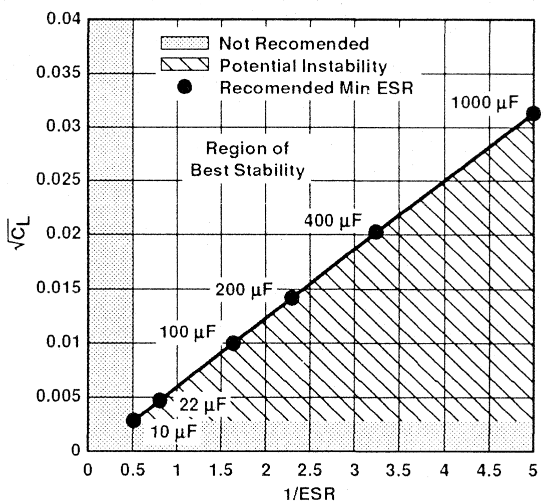
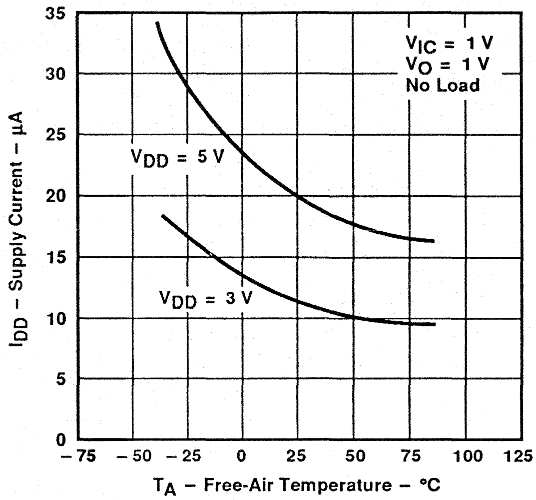


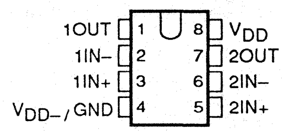
Figure 4

- Wide Range of Supply Voltages Over Specified Temperature Range: T_A = − 40°C to 85°C . . . 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} − 1 V at T_A = 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

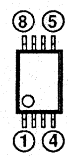
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TLV2322 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage single-supply applications. This amplifier is especially well suited to ultra-low power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V of the positive rail.

These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier is specified at only 27 µA over its full temperature range of − 40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon gate LinCMOS™ technology. The LinCMOS process also features extremely high

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
− 40°C to 85°C	9 mV	TLV2322ID	TLV2322IP	TLV2322IPW	TLV2322Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2322IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2322IPWLE).

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description (continued)

input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

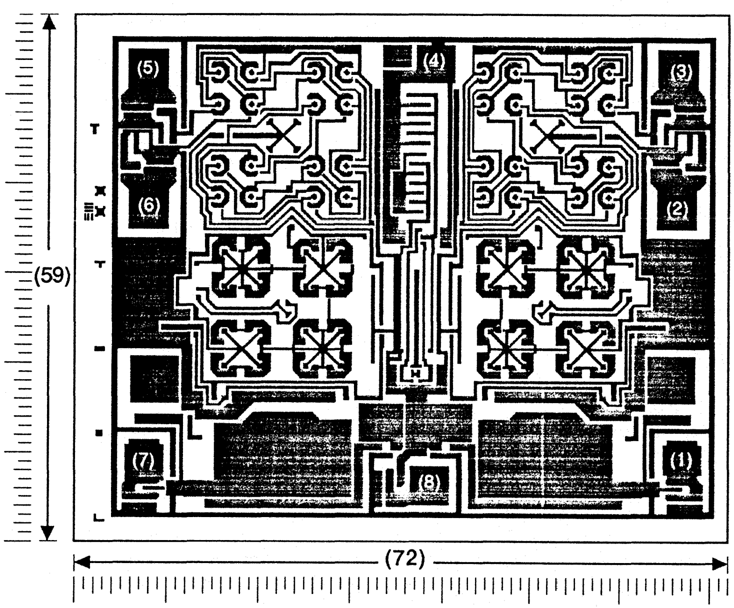
To facilitate the design of small portable equipment, the TLV2322 is made available in a wide range of package options, including the small-outline and thin-scaled-small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

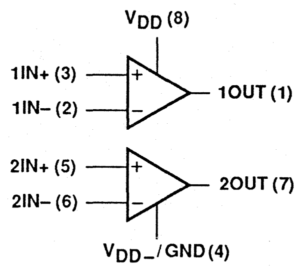
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2322 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2322Y chip information

These chips, properly assembled, display characteristics similar to the TLV2322I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

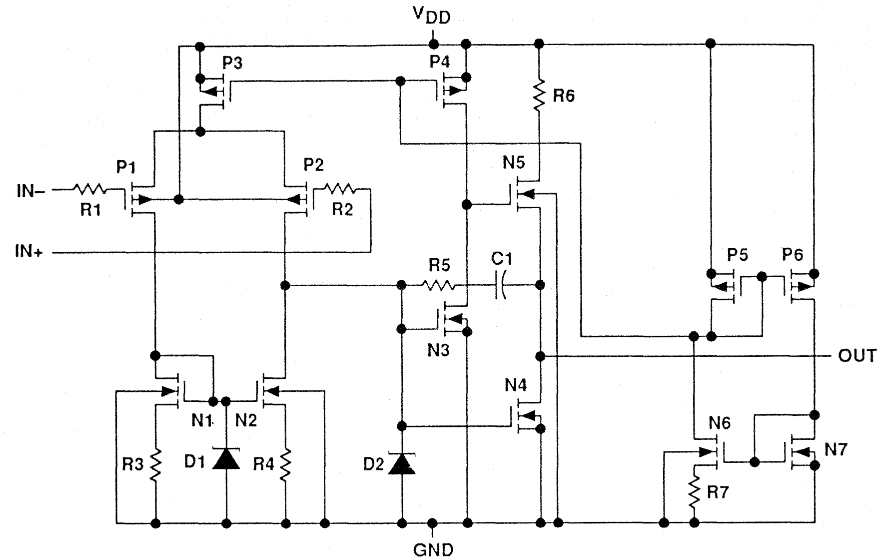
TOLERANCES
ARE ± 10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)

COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

†Includes both amplifiers and all ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage (see Note 2)	$\pm V_{DD}$
Input voltage range, V_I (any input)	-0.3 V to V_{DD}
Input current, I_I	± 5 mA
Output current, I_O	± 30 mA
Duration of short-circuit current at (or below) $T_A = 25°C$ (see Note 3)	Unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	$-40°C$ to $85°C$
Storage temperature range	$-65°C$ to $150°C$
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package	260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	– 0.2	1.8	V
	$V_{DD} = 5$ V	– 0.2	3.8	
Operating free-air temperature, T_A		– 40	85	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V MIN	V_{DD} = 3 V TYP	V_{DD} = 3 V MAX	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	– 0.2 to 2	– 0.3 to 2.3		– 0.2 to 4	– 0.3 to 4.2		V
			Full range	– 0.2 to 1.8			– 0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = –1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = – 100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		12	34		20	34	µA
			Full range			54			54	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_{OPP} = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 30		25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 30		25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		−40°C		38°		
				25°C		34°		
				85°C		28°		

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ		1.1	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	86		70	86		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		12	34		20	34	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Gain-bandwidth product	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE

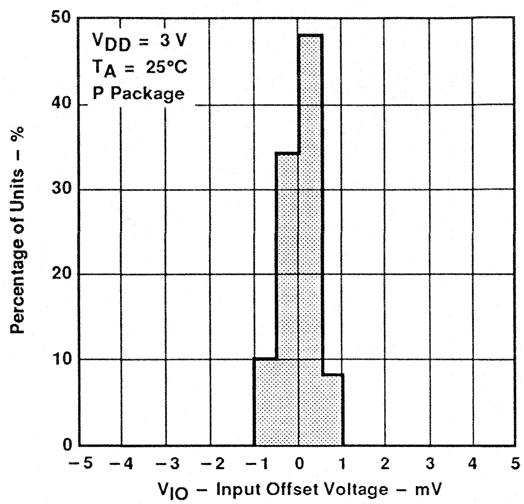


Figure 1

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE

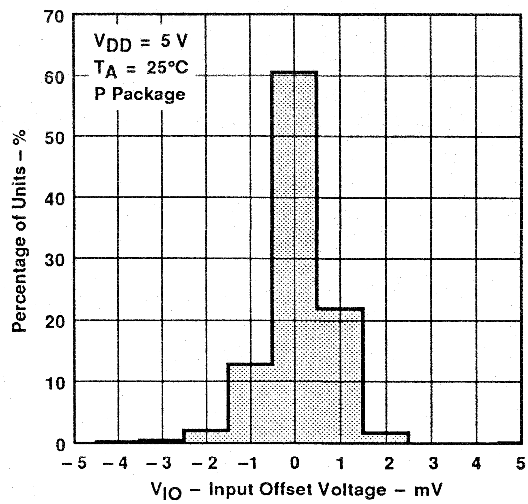


Figure 2

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

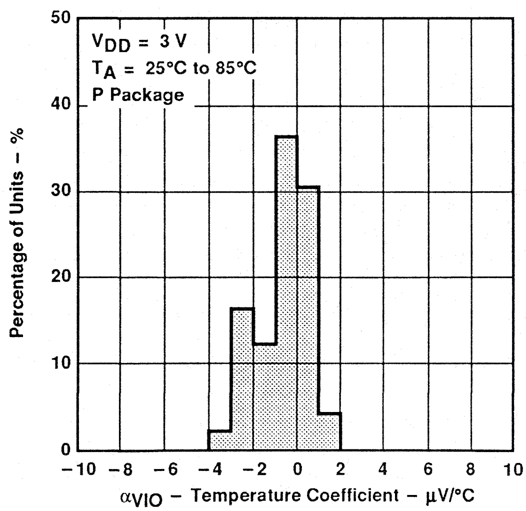


Figure 3

DISTRIBUTION OF TLV2322
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

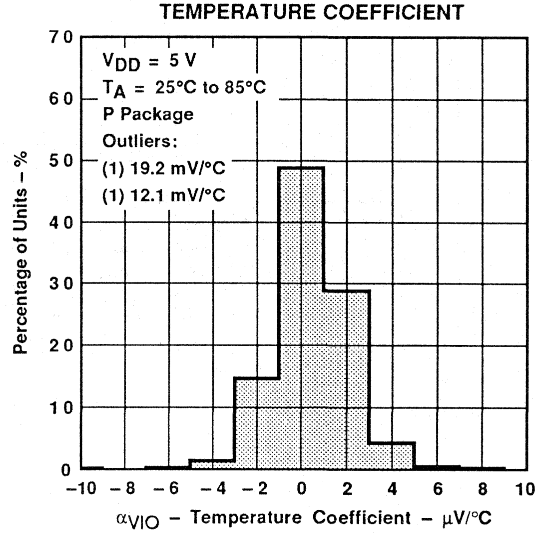


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

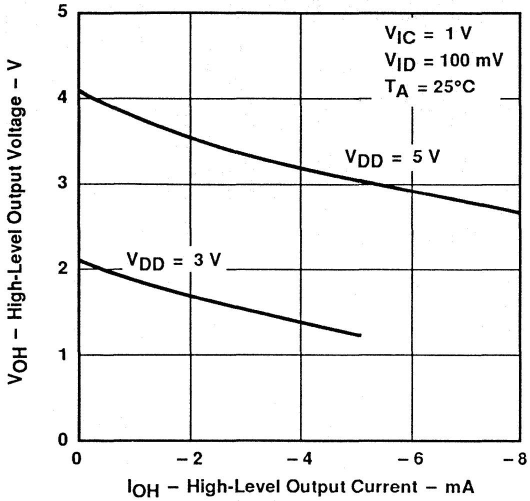


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

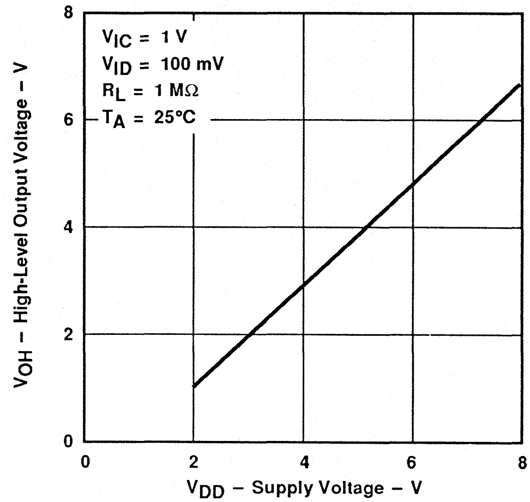


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

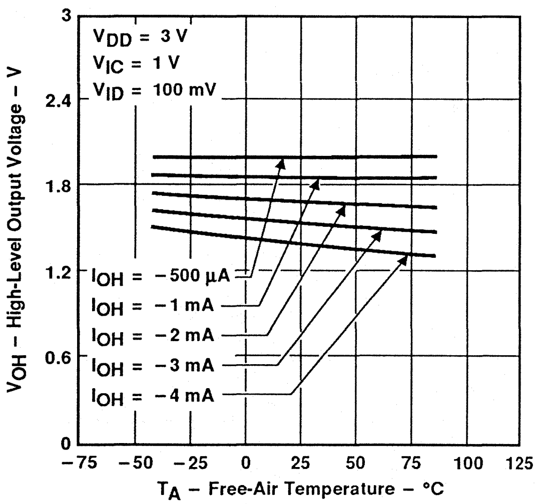


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

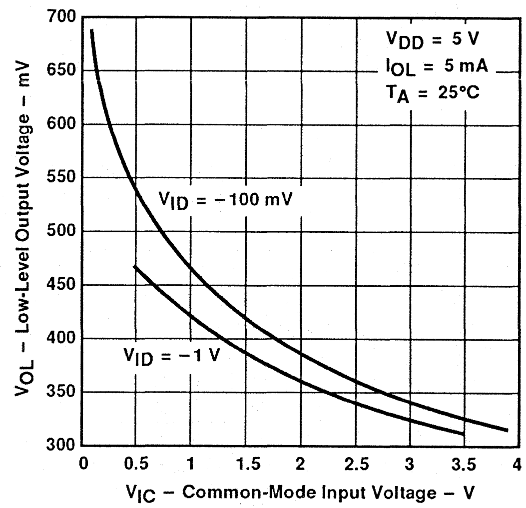


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

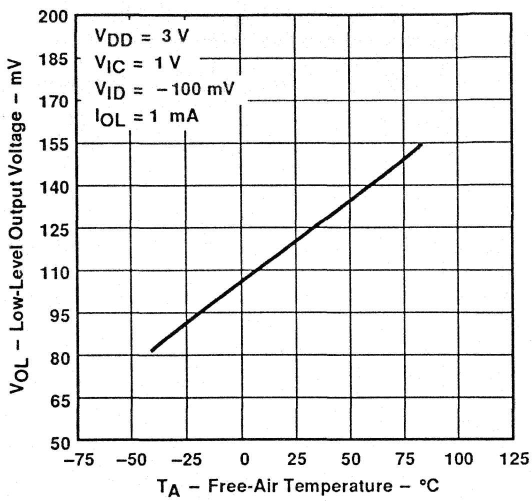


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

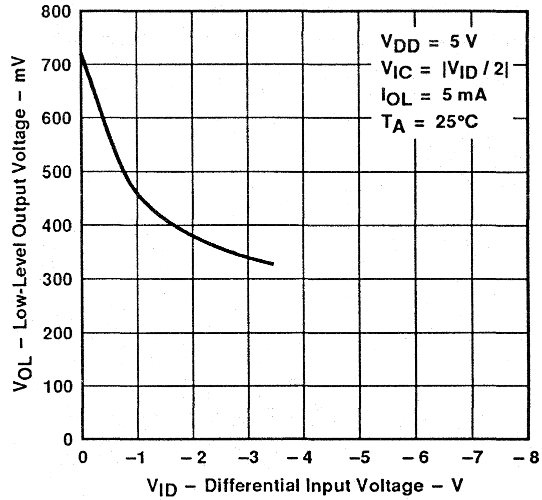


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

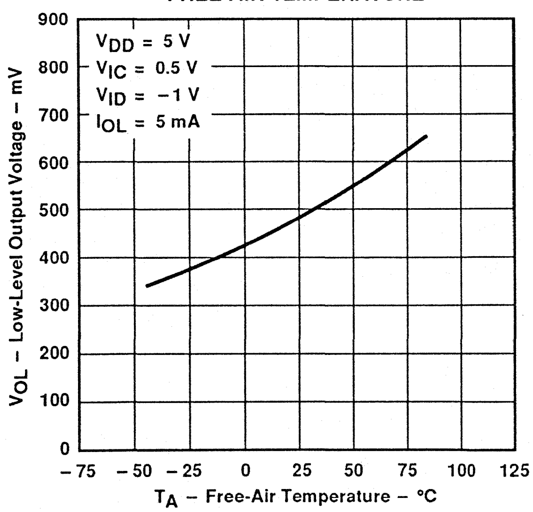


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

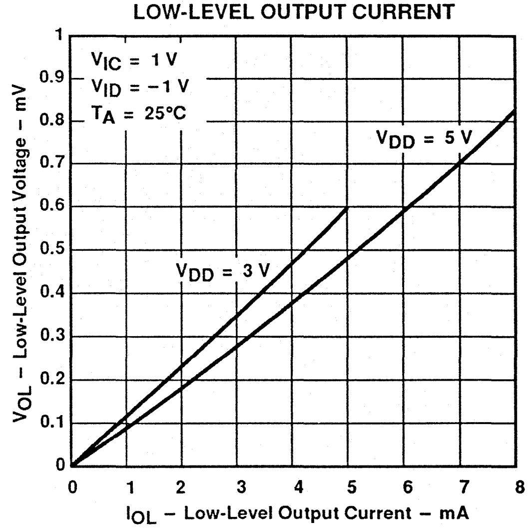


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

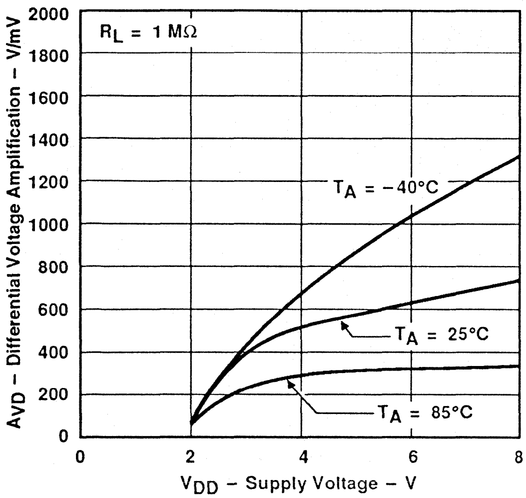


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

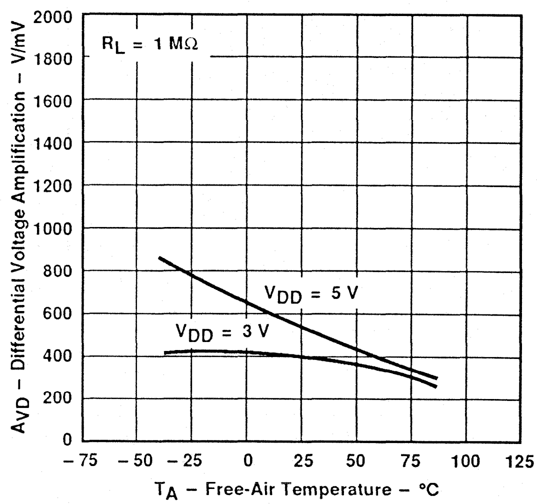


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

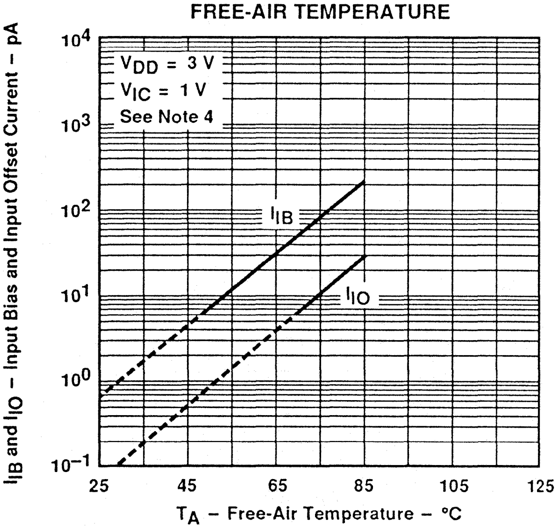


Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

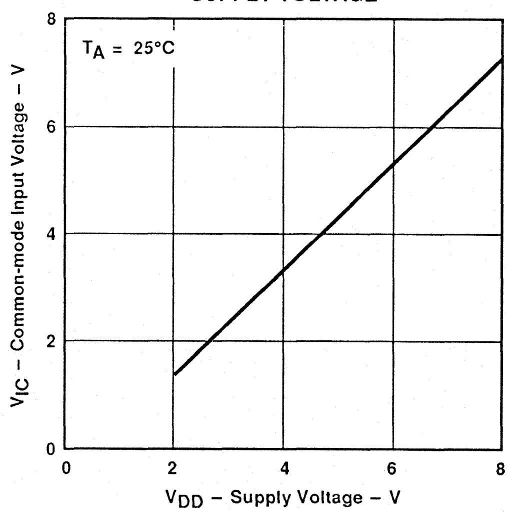


Figure 16

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

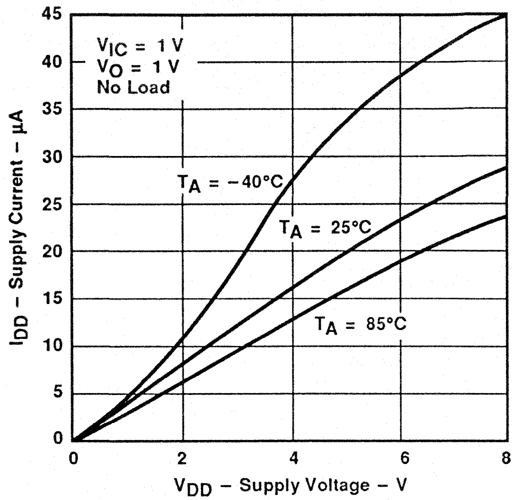


Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

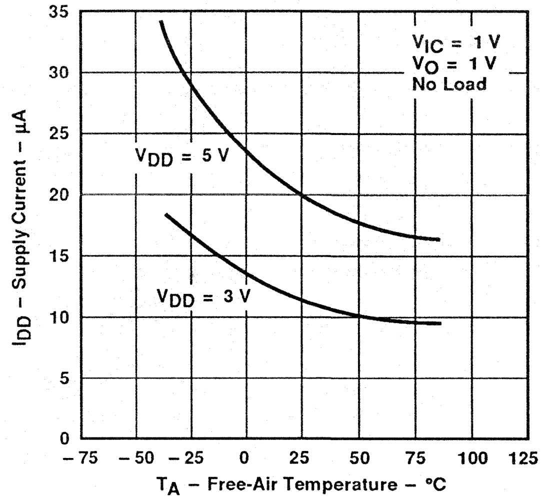


Figure 18

SLEW RATE
vs
SUPPLY VOLTAGE

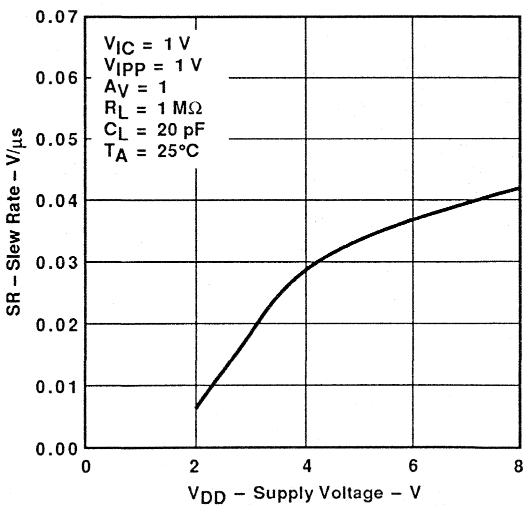


Figure 19

SLEW RATE
vs
FREE-AIR TEMPERATURE

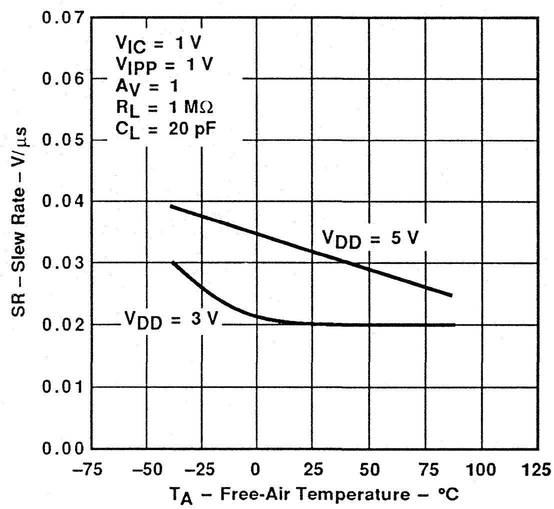


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

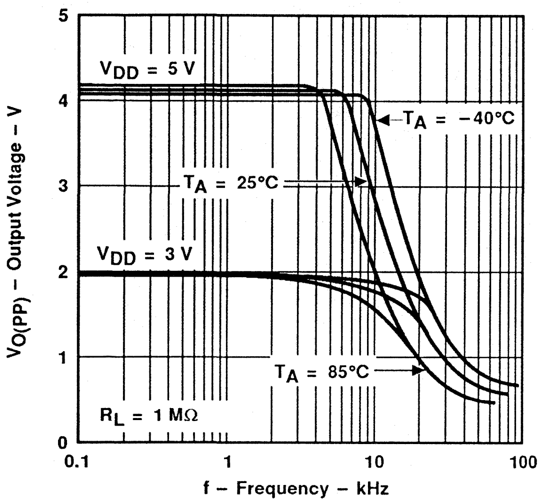


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

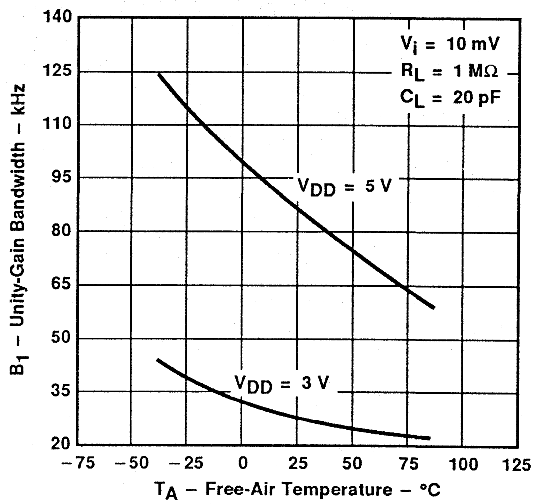


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

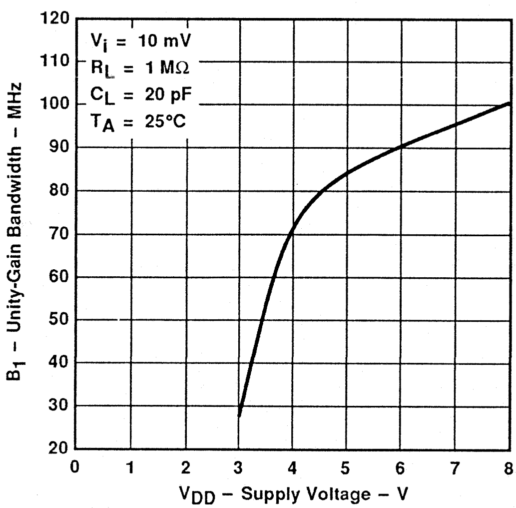


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

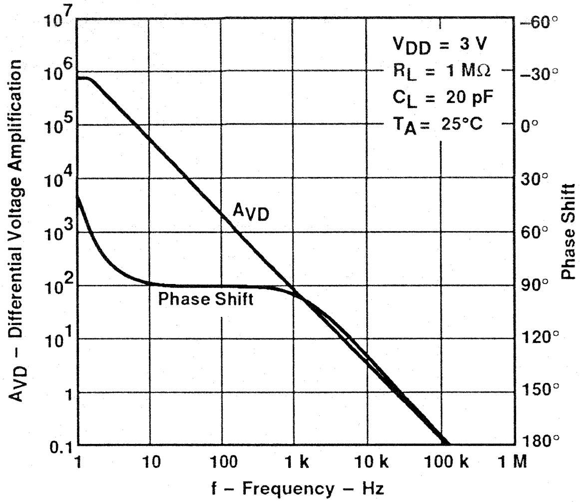


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

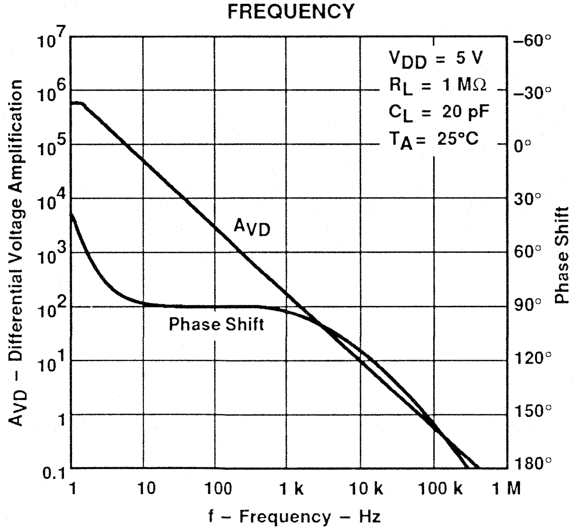


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

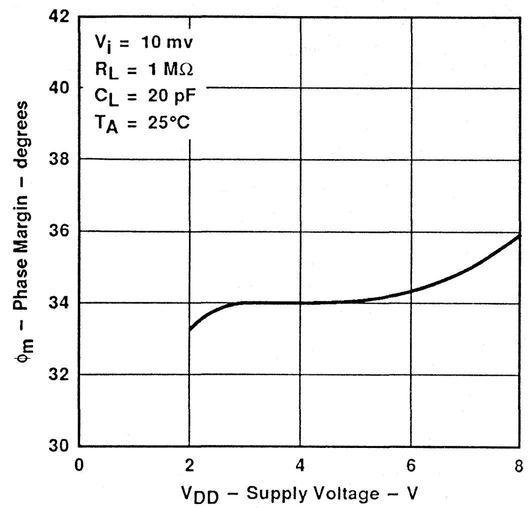


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

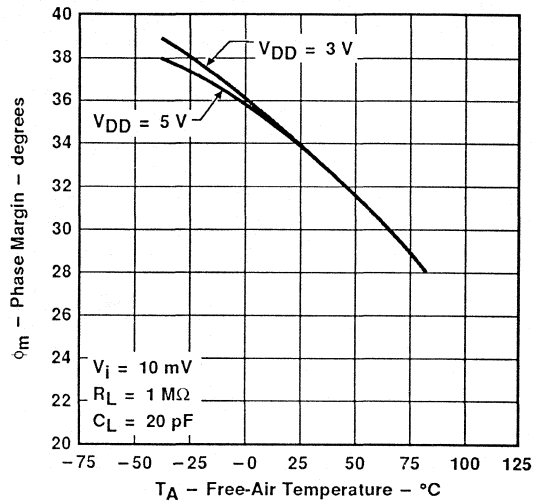


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

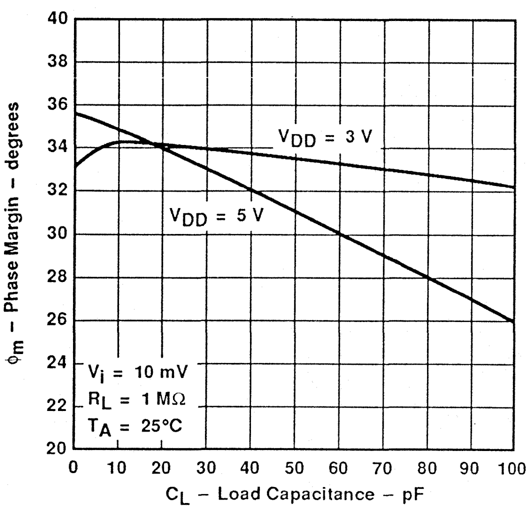


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

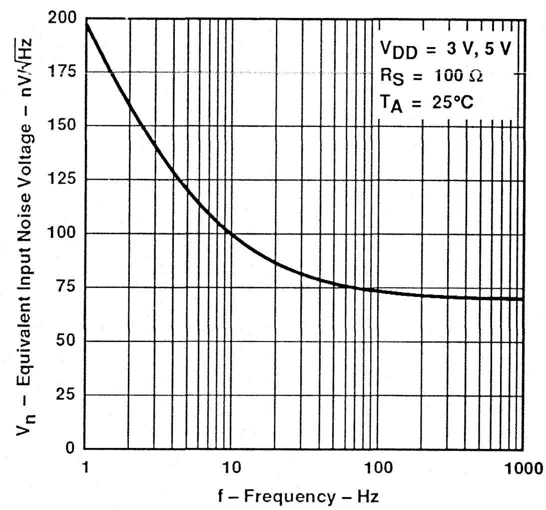
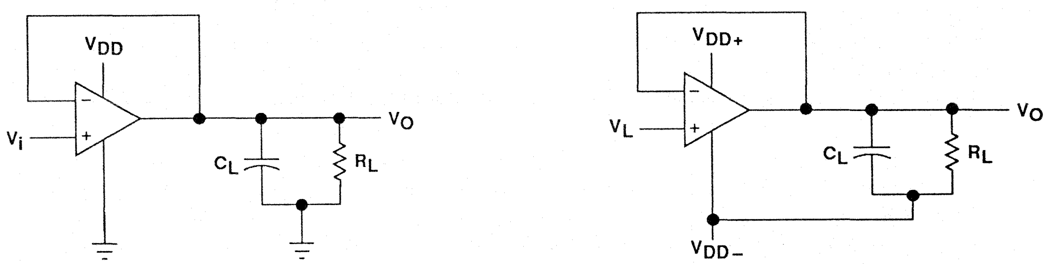


Figure 29

PARAMETER MEASUREMENT INFORMATION

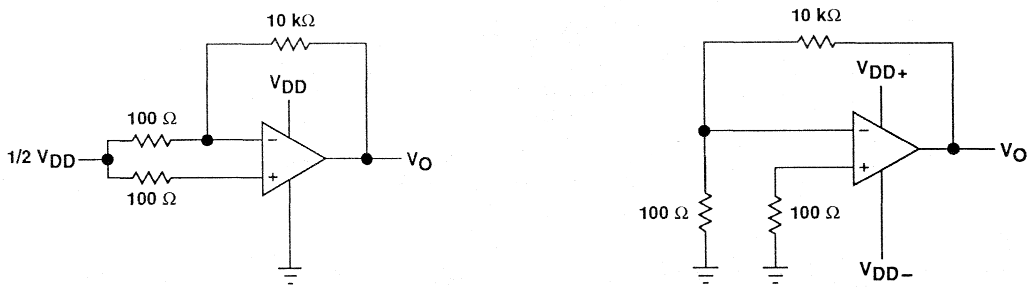
single-supply versus split-supply test circuits

Because the TLV2322 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



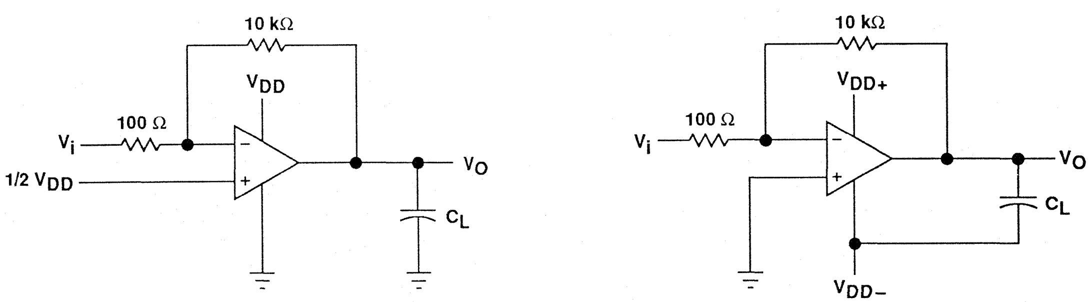
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2322 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

   One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

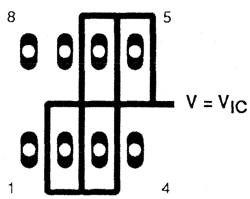


Figure 33. Isolation Metal Around Device Inputs (P Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

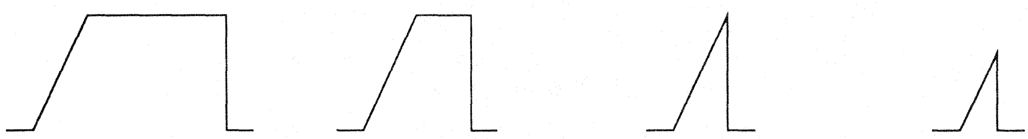


Figure 34. Full-Power-Response Output Signal

test time

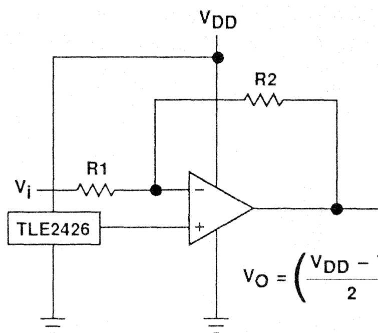
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLV2322 will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.



$$V_O = \left(\frac{V_{DD} - V_i}{2}\right)\frac{R_2}{R_1} + \frac{V_{DD}}{2}$$

Figure 35. Inverting Amplifier With Voltage Reference

TYPICAL APPLICATION DATA

The TLV2322 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.

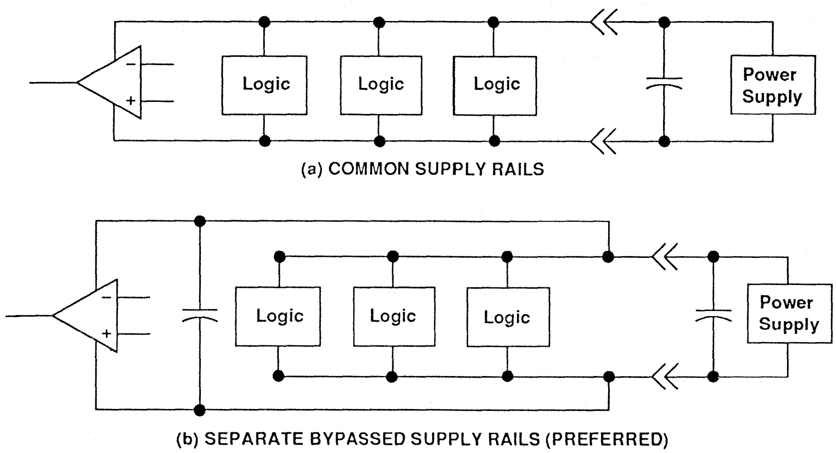


Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2322 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2322 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLV2322 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

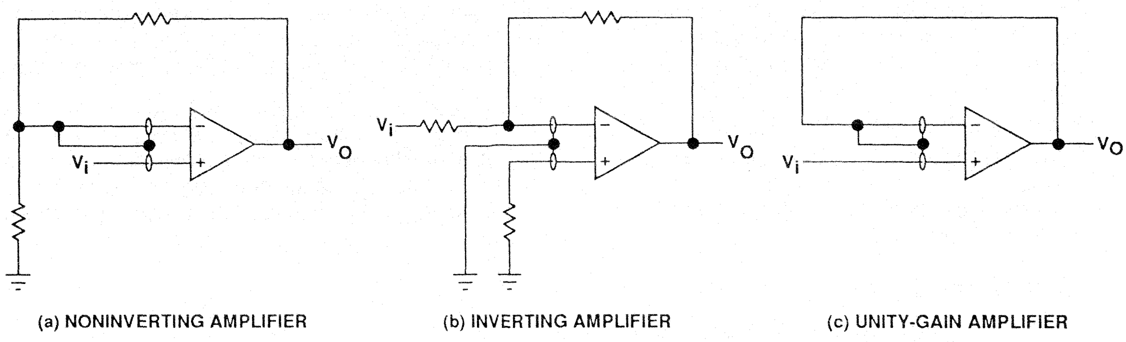


Figure 37. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2322 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

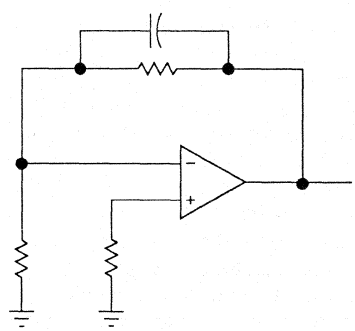


Figure 38. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2322 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2322 inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

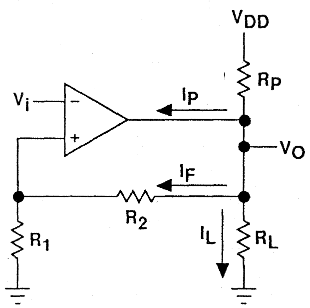
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2322 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2322 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2322 are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 41, 42, and 43). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 µA)

Figure 39. Resistive Pullup to Increase V_{OH}

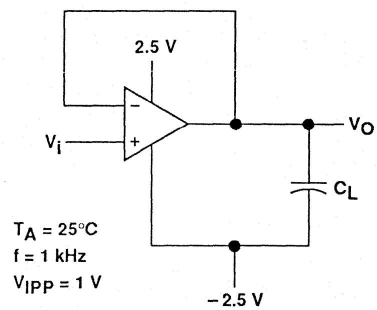
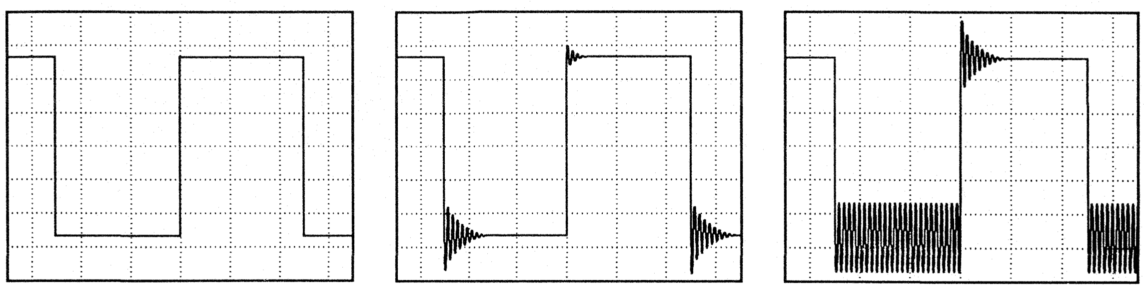


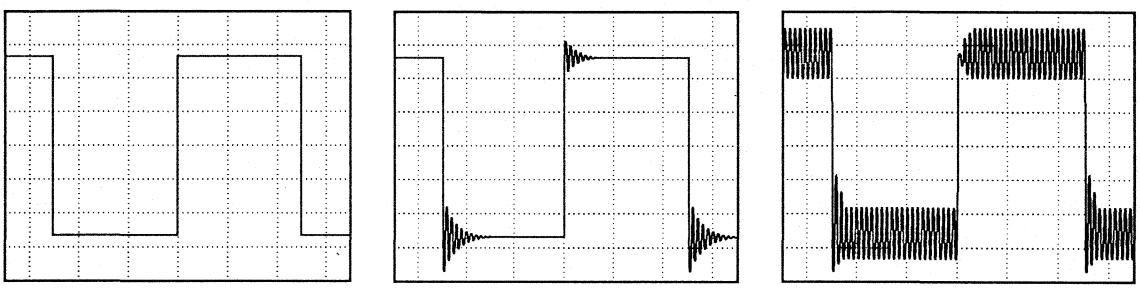
Figure 40. Test Circuit for Output Characteristics

TYPICAL APPLICATION DATA



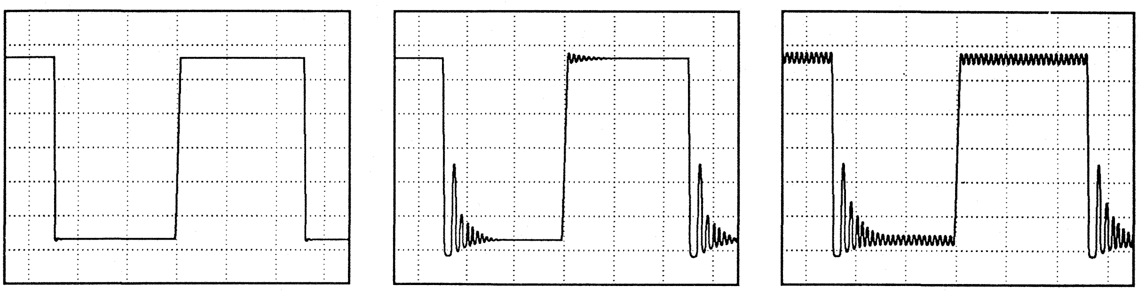
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 42. Effect of Capacitive Loads in Medium-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 43. Effect of Capacitive Loads in Low-Bias Mode

- Wide Range of Supply Voltages Over Specified Temperature Range: T_A = −40°C to 85°C . . . 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} − 1 V at 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

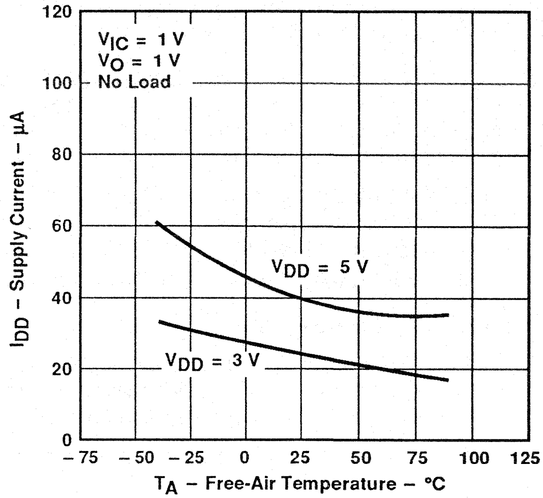
description

The TLV2324 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. This amplifier is especially well suited to ultra-low power systems that require devices to consume the absolute minimum of supply currents. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input-voltage range includes the negative rail and extends to within 1 V from the positive rail.

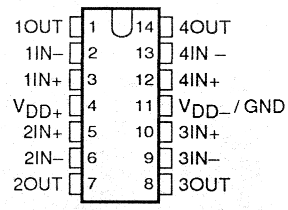
These amplifiers are specifically targeted for use in very low-power, portable, battery-driven applications with the maximum supply current per operational amplifier specified at only 27 µA over its full temperature range of −40°C to 85°C.

Low-voltage and low-power operation has been made possible by using the Texas Instruments

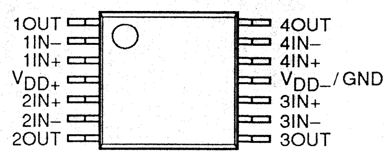
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
−40°C to 85°C	10 mV	TLV2324ID	TLV2324IN	TLV2324IPW	TLV2324Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2324IDR). The PW package is only available left-end taped and reeled (e.g., TLV2324IPWLE).

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TEXAS INSTRUMENTS

description (continued)

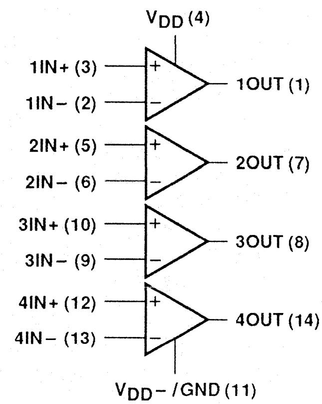
silicon gate, LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV2324 is made available in a wide range of package options, including the small-outline and thin-scaled-small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

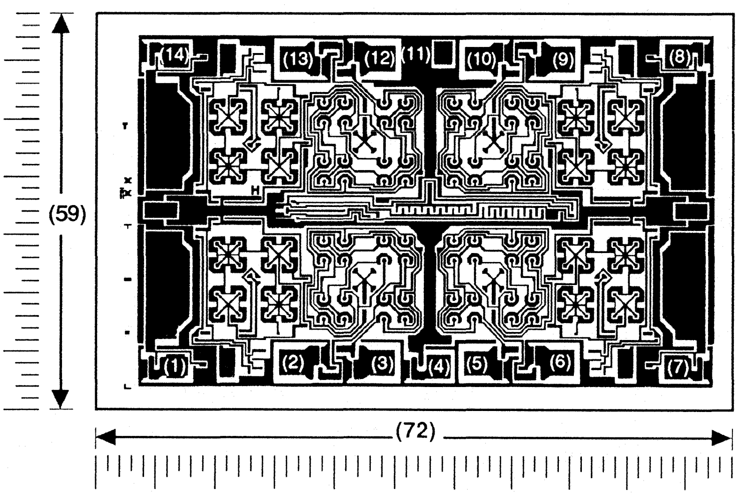
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2324 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2324Y chip information

These chips, properly assembled, display characteristics similar to the TLV2324I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



BONDING PAD ASSIGNMENTS



CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

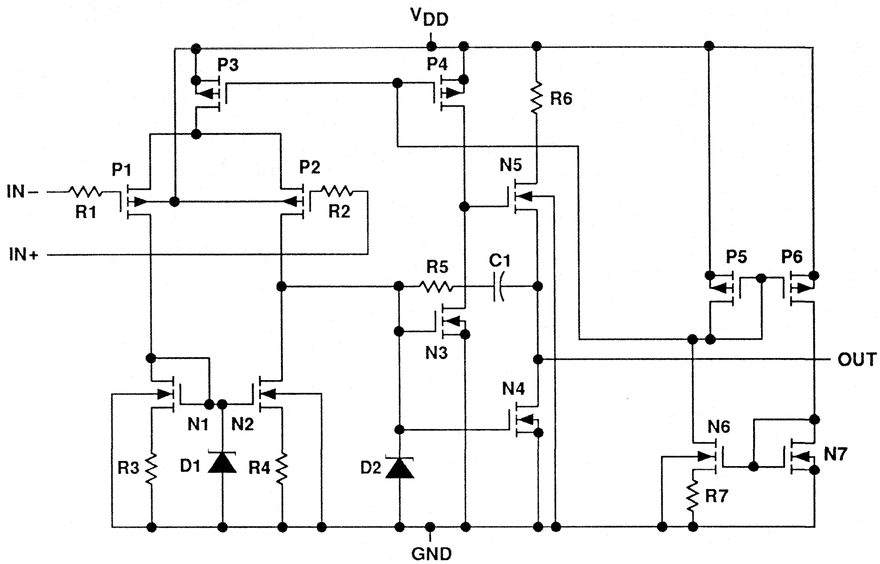
TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)

COMPONENT COUNT†	
Transistors	108
Diodes	8
Resistors	28
Capacitors	4

†Includes all amplifiers, ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . 8 V
Differential input voltage (see Note 2) . . . . ± V_{DD}
Input voltage range, V_I (any input) . . . . – 0.3 V to V_{DD}
Input current, I_I . . . . ± 5 mA
Output current, I_O . . . . ± 30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . . Unlimited
Continuous total dissipation . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . – 40°C to 85°C
Storage temperature range . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package . . . . 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1575 mW	12.6 mW/°C	819 mW
PW	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	−0.2	1.8	V
	$V_{DD} = 5$ V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V MIN	V_{DD} = 3 V TYP	V_{DD} = 3 V MAX	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		24	68		39	68	μA
			Full range			108			108	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_{OPP} = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 30		25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 30		25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 1 MΩ, See Figure 32		−40°C		38°		
				25°C		34°		
				85°C		28°		

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1MΩ		1.1	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	86		70	86		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		24	68		39	68	µA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Gain-bandwidth product	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE

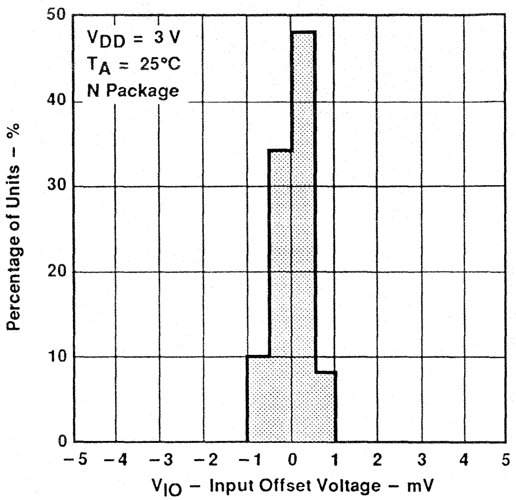


Figure 1

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE

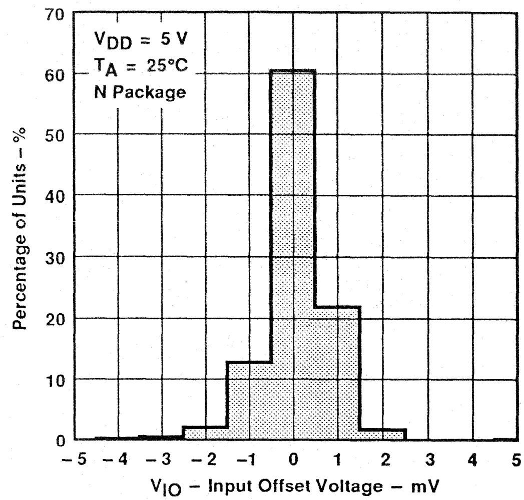


Figure 2

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

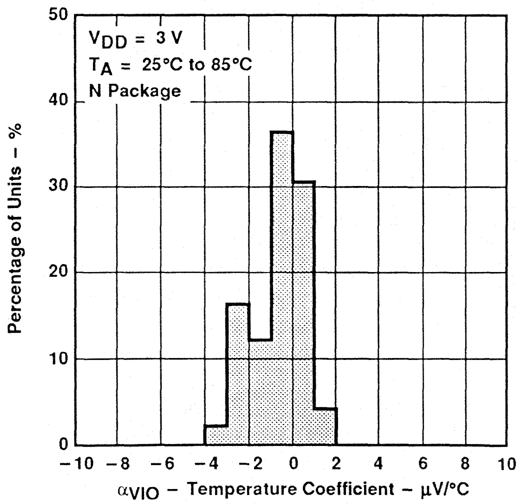


Figure 3

DISTRIBUTION OF TLV2324
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

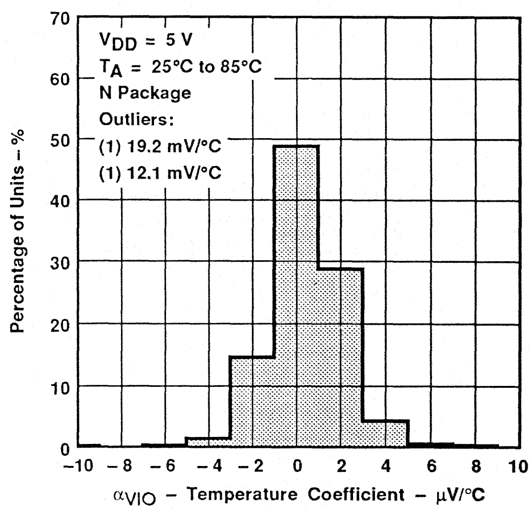


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

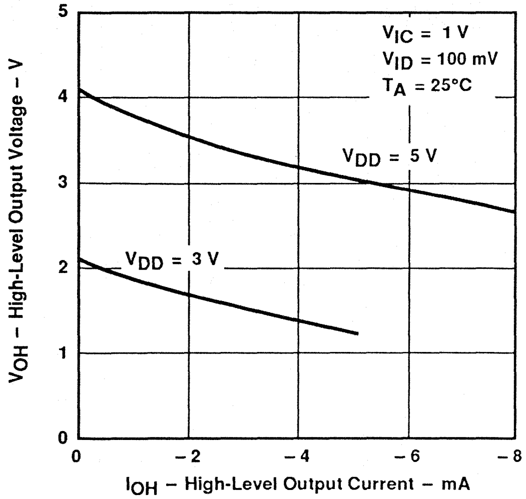


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

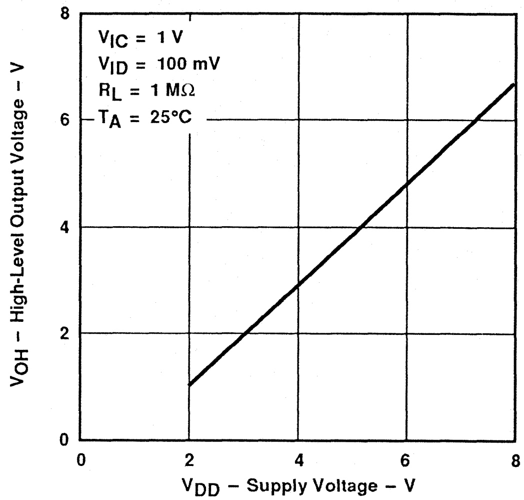


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

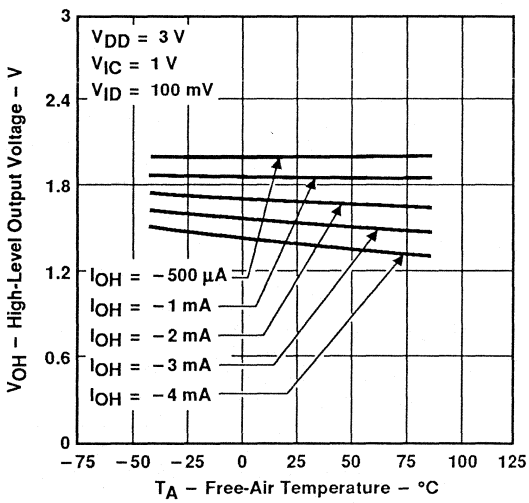


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

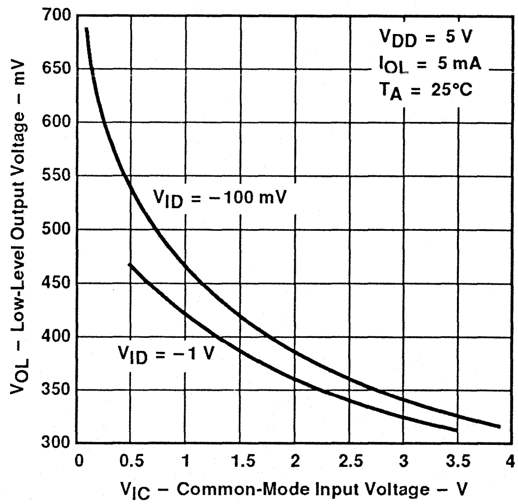


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

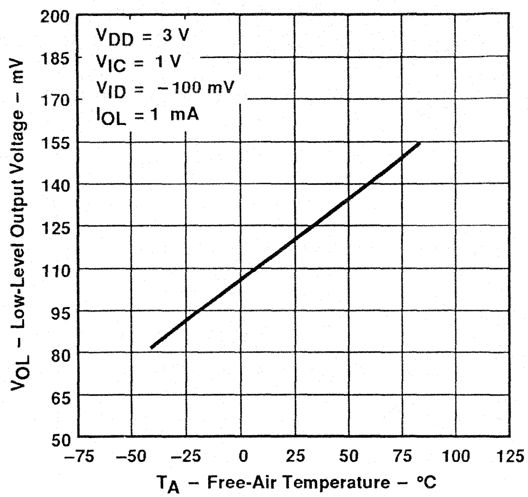


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

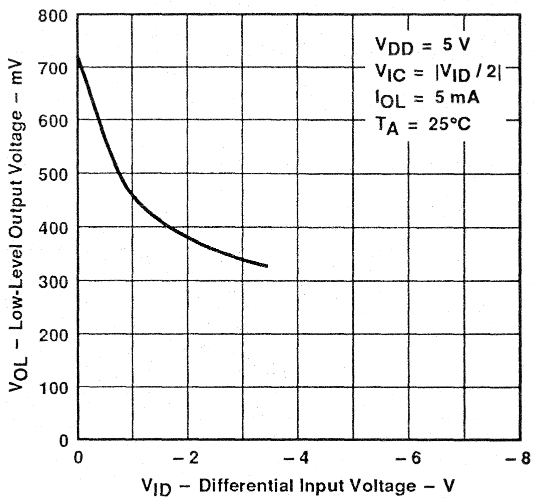


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

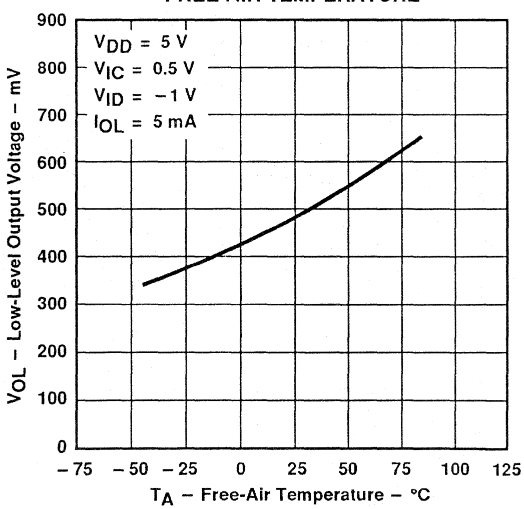


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

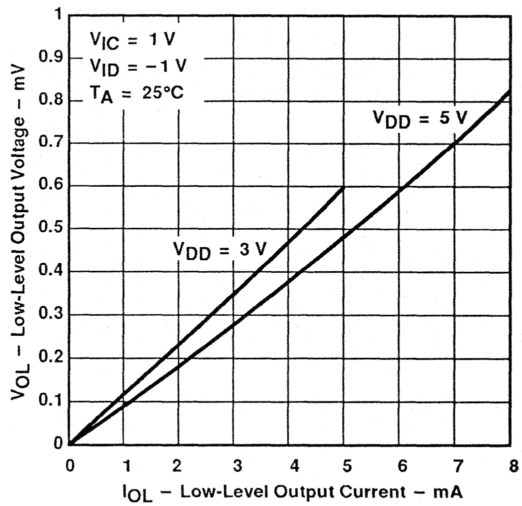


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

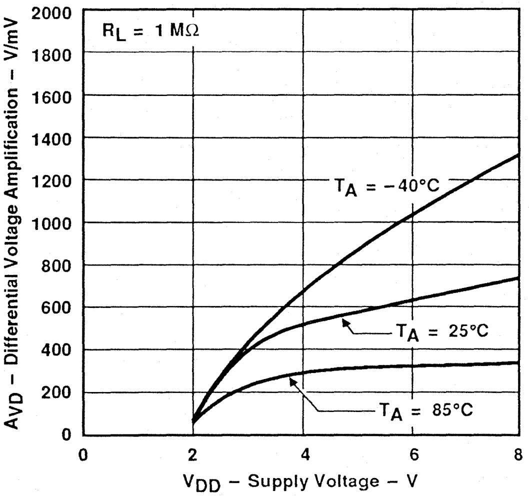


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

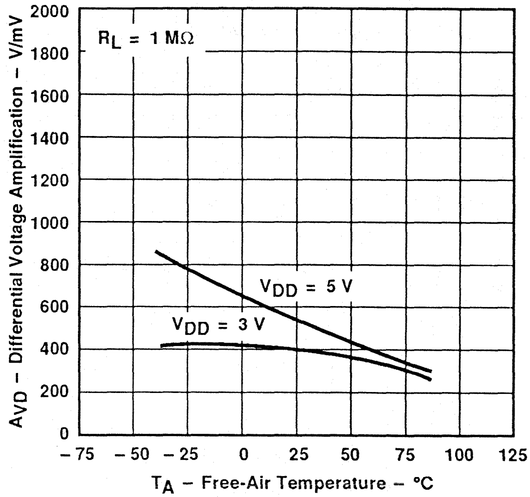


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

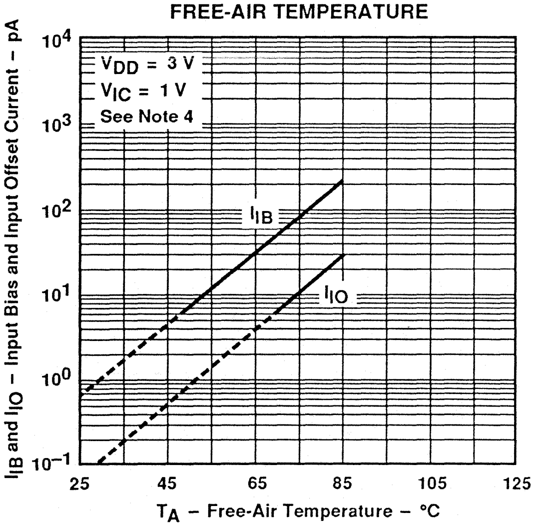


Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

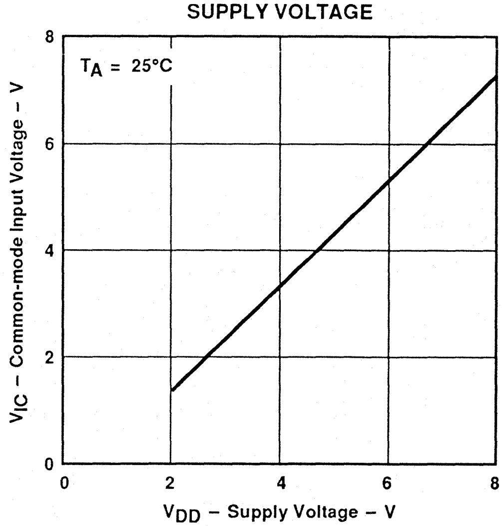


Figure 16

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

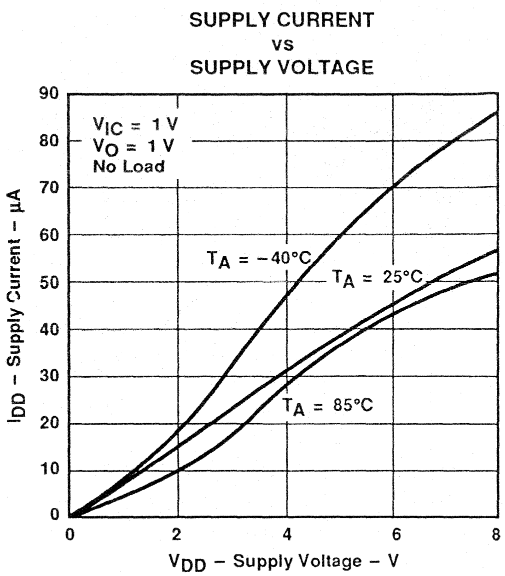


Figure 17

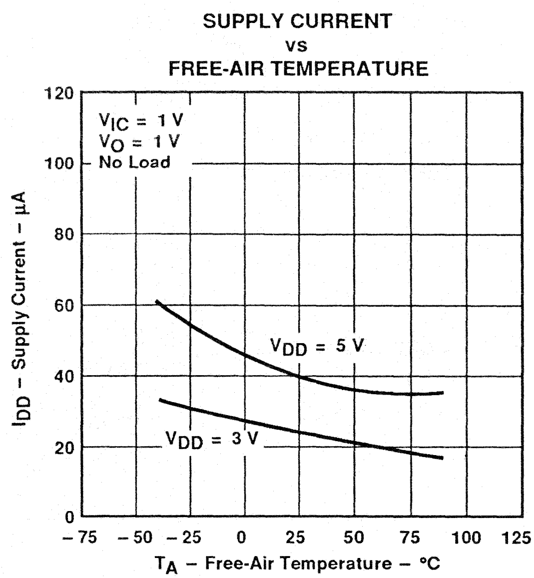


Figure 18

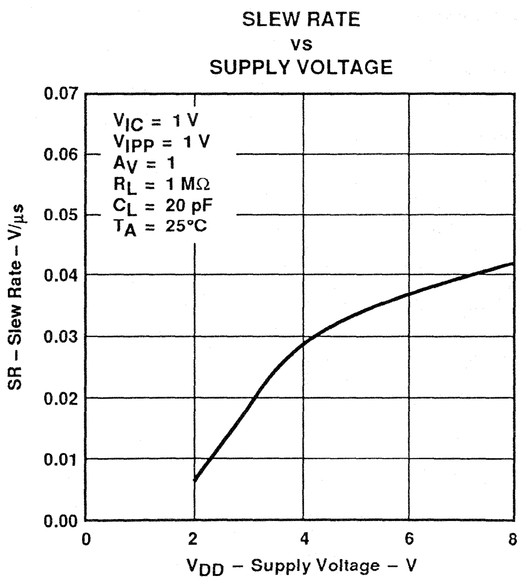


Figure 19

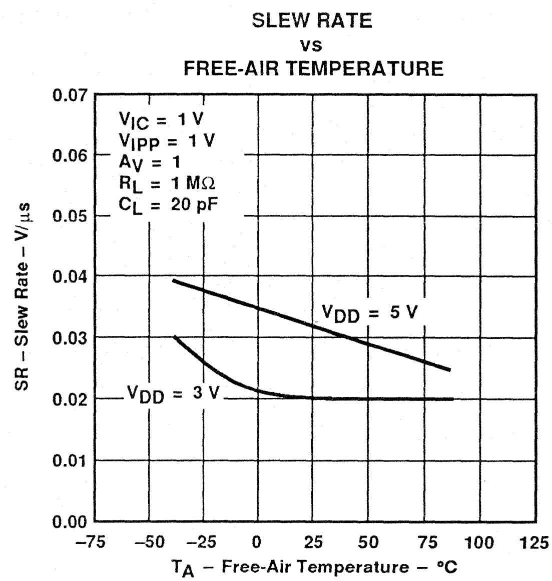


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

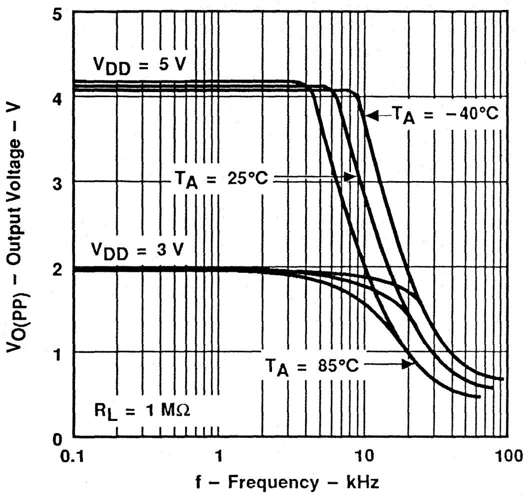


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

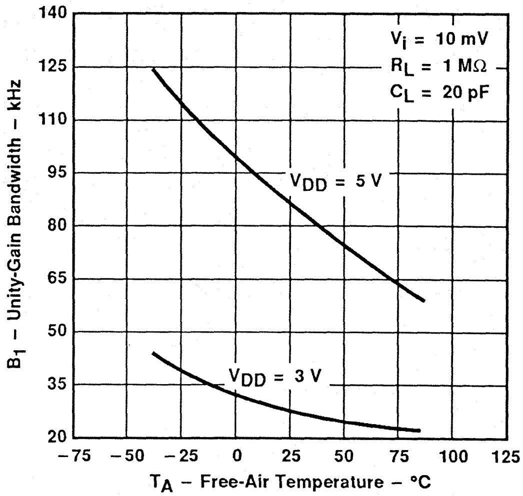


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

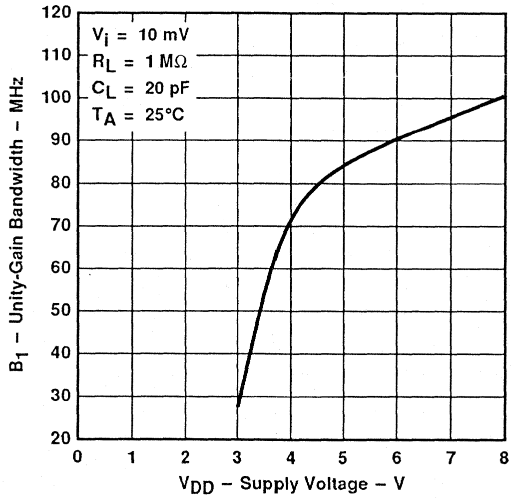


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

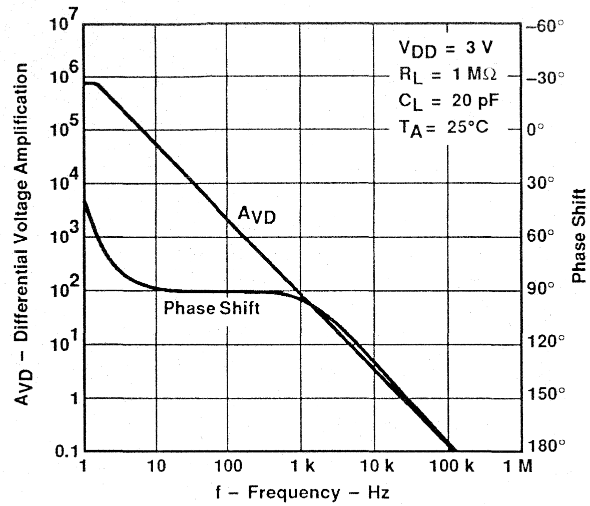


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

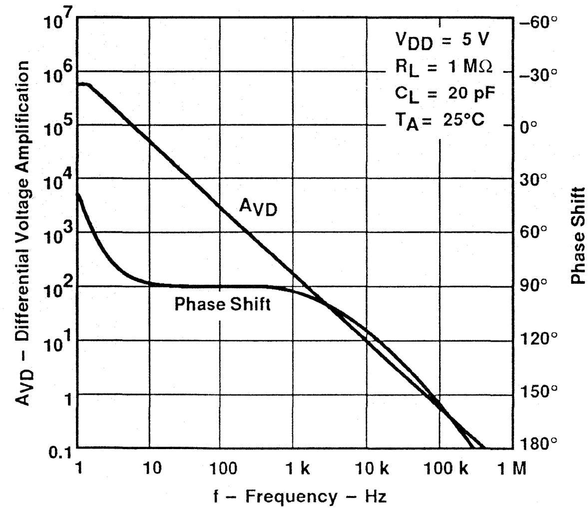


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

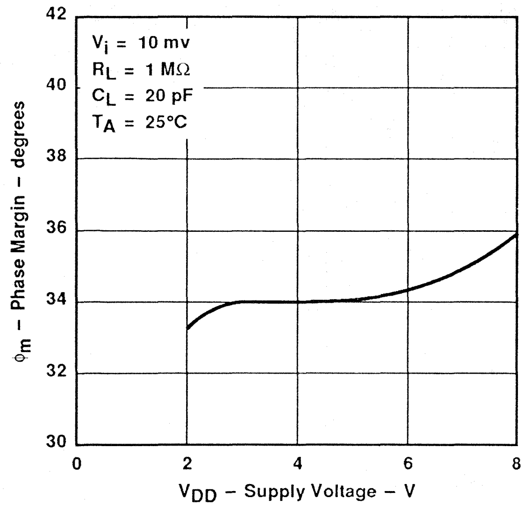


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

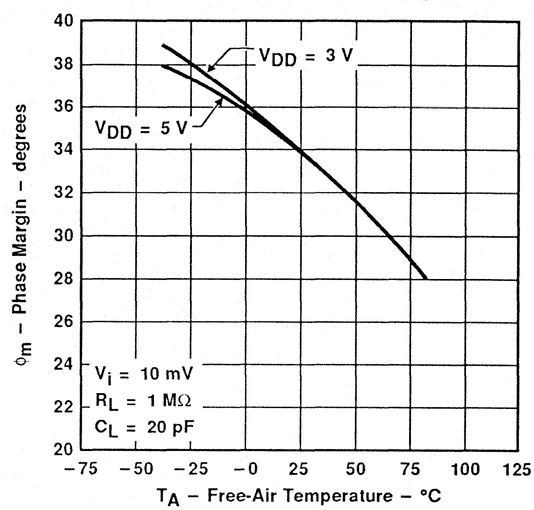


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

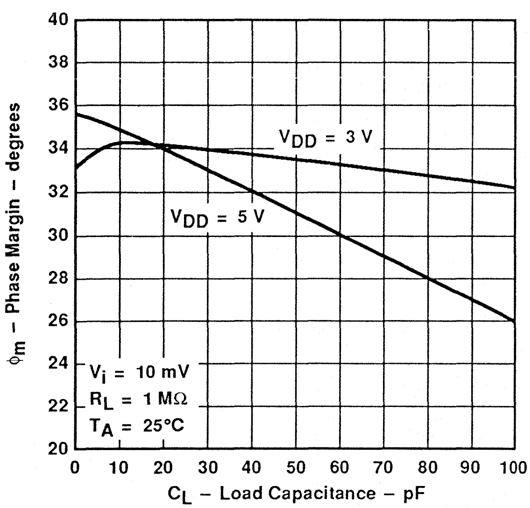


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

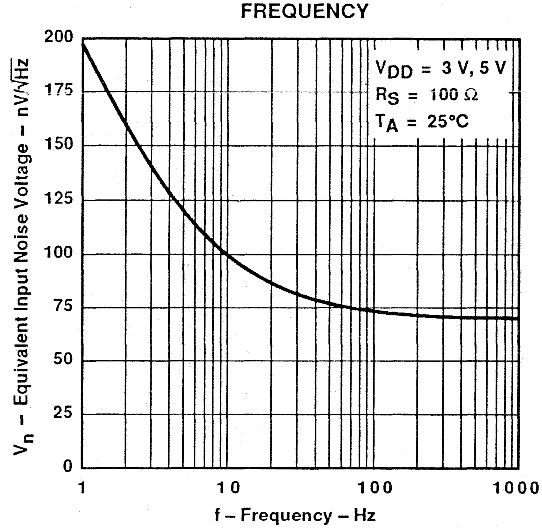
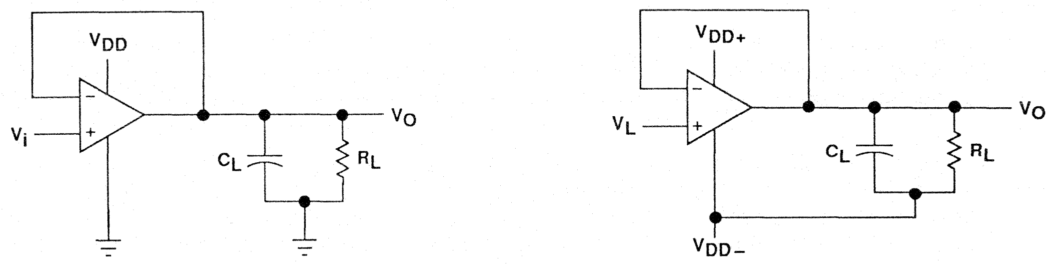


Figure 29

PARAMETER MEASUREMENT INFORMATION

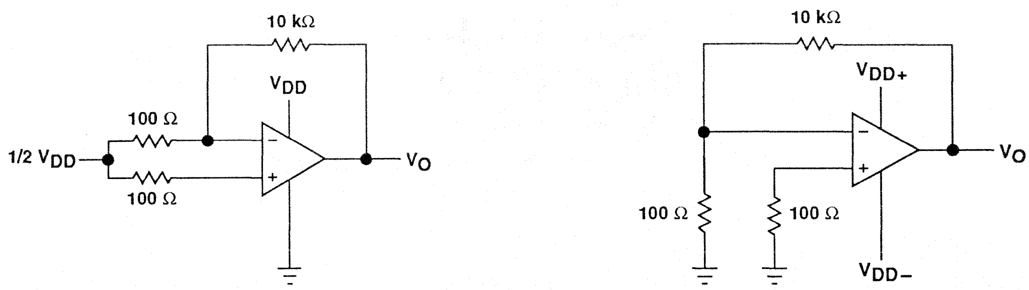
single-supply versus split-supply test circuits

Because the TLV2324 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



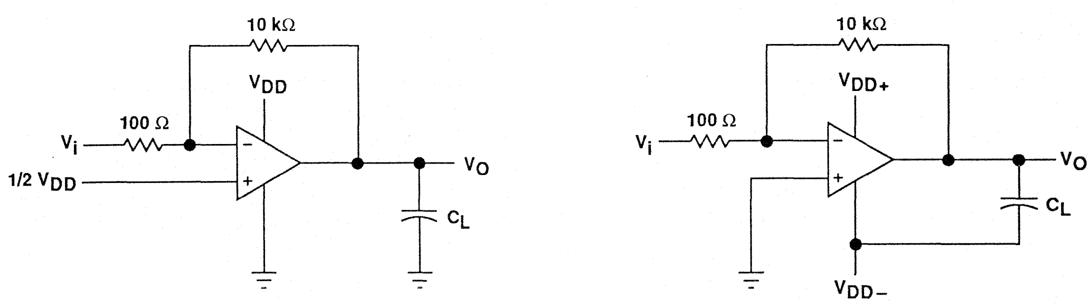
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2324 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

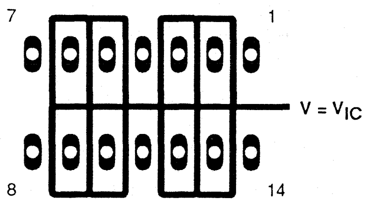


Figure 33. Isolation Metal Around Device Inputs (N Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

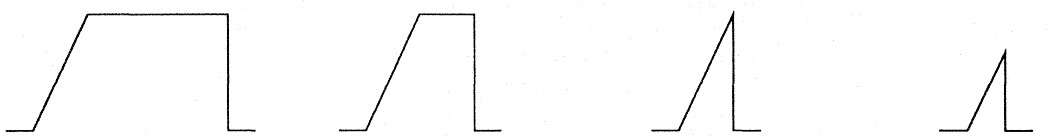


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

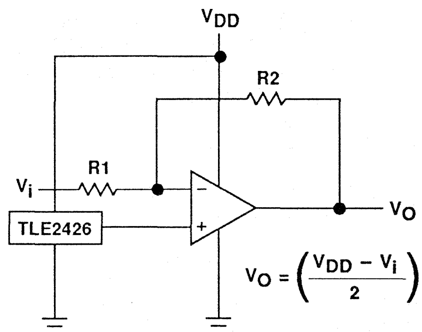
TYPICAL APPLICATION DATA

single-supply operation

While the TLV2324 will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.

The TLV2324 works well in conjunction with



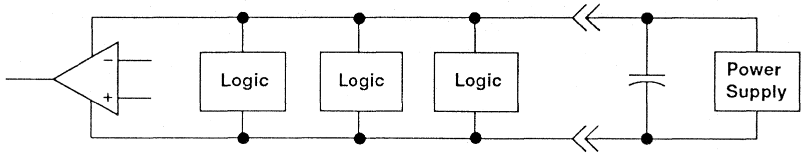
$$V_O = \left(\frac{V_{DD} - V_I}{2}\right)\frac{R_2}{R_1} + \frac{V_{DD}}{2}$$

Figure 35. Inverting Amplifier With Voltage Reference

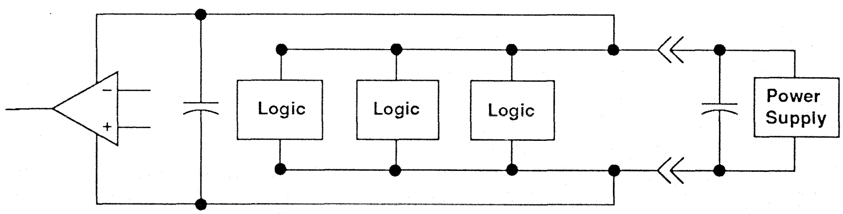
TYPICAL APPLICATION DATA

digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2324 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2324 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLV2324 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

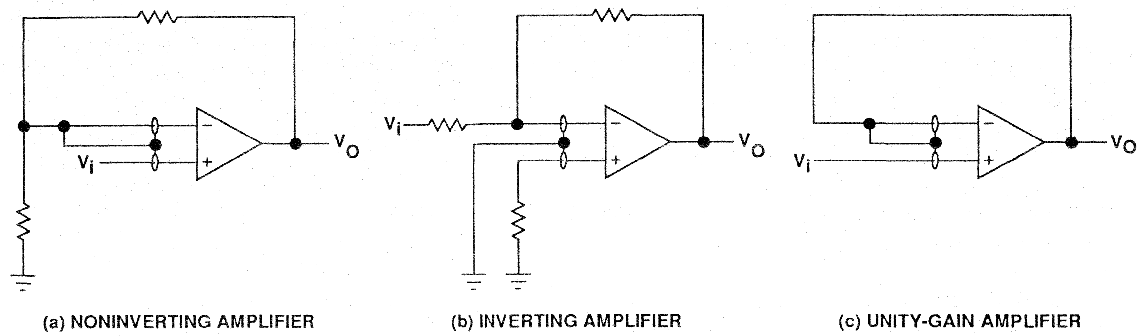


Figure 37. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2324 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

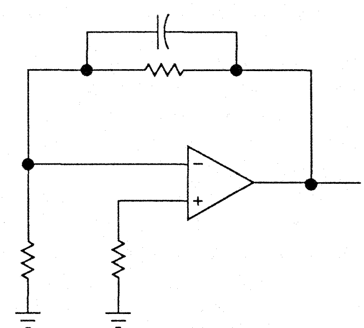


Figure 38. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2324 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2324 inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

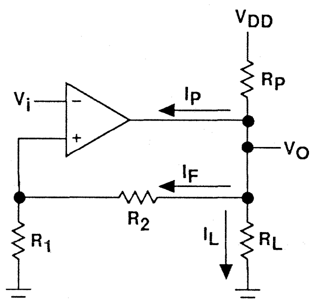
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2324 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2324 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2324 are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 41, 42, and 43). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 µA)

Figure 39. Resistive Pullup to Increase V_{OH}

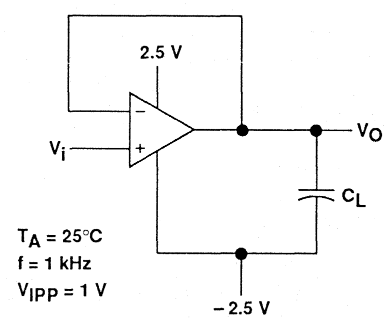
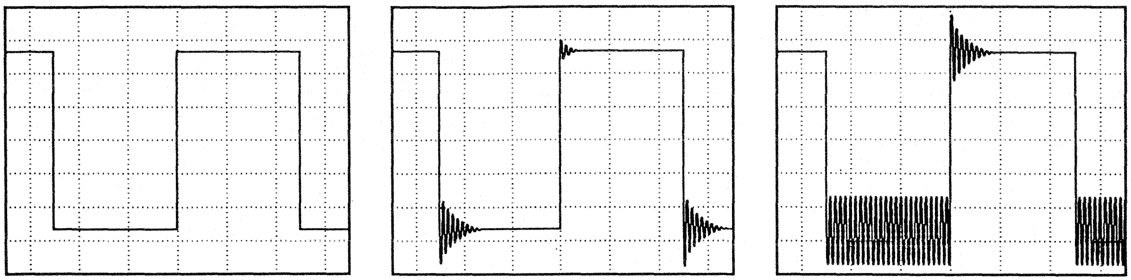


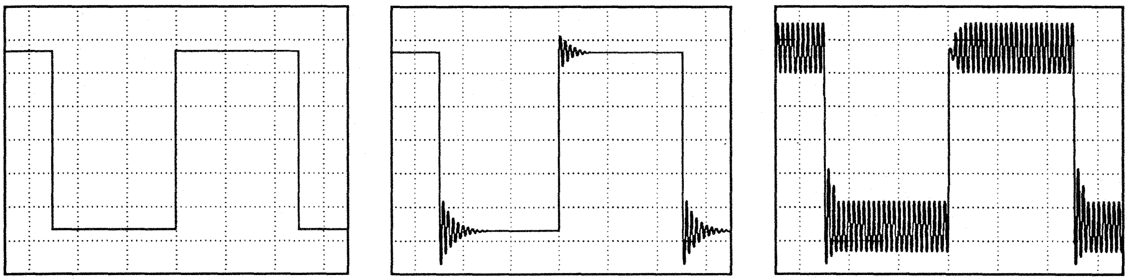
Figure 40. Test Circuit for OutputCharacteristics

TYPICAL APPLICATION DATA



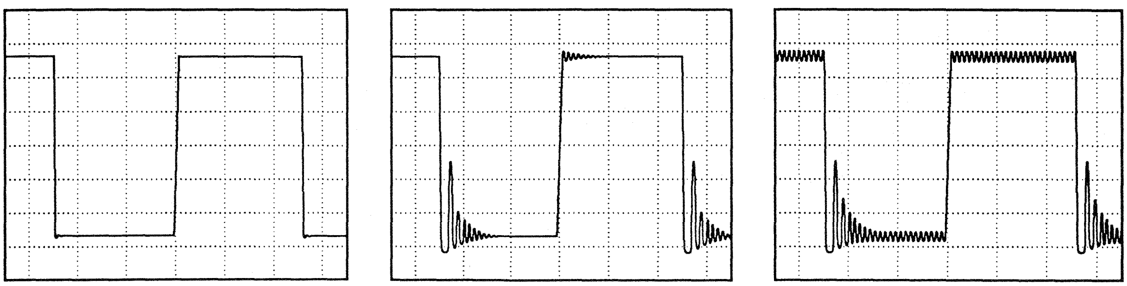
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 42. Effect of Capacitive Loads in Medium-Bias Mode

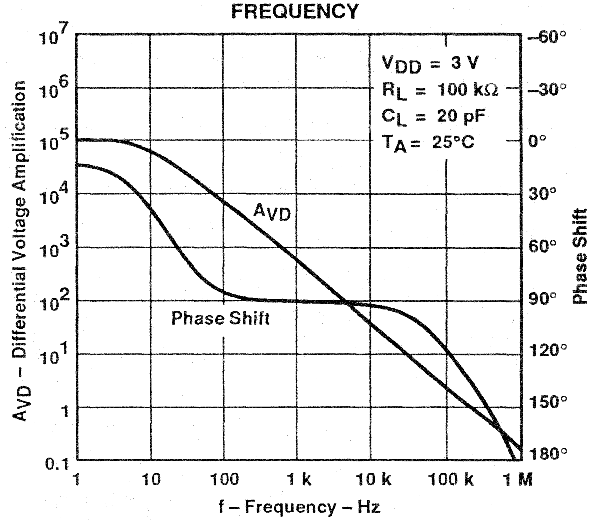


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 43. Effect of Capacitive Loads in Low-Bias Mode

- Wide Range of Supply Voltages Over Specified Temperature Range: T_A = −40°C to 85°C . . . 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} − 1 V at T_A = 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

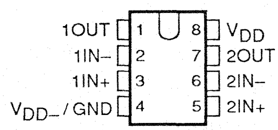
LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY



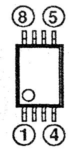
description

The TLV2332 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike the TLV2322 which is optimized for ultra-low power, the TLV2332 is designed to provide a combintion of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

D OR P PACKAGE (TOP VIEW)



PW PACKAGE (TOP VIEW)



Having a maximum supply current of only 310 µA per amplifier over full termperature range, the TLV2332 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifiers typical slew rate is 0.38 V/µs and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels. The TLV2332 operational amplifiers are especially well suited for use in low current or battery-powered applications.

Low-voltage and low-power operation has been made possible by using the Texas Instruments silicon gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low bias currents making these amplifiers ideal for interfacing to high-impedance sources such as sensor circuits or filter applications.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
−40°C to 85°C	9 mV	TLV2332ID	TLV2332IP	TLV2332IPW	TLV2332Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2332IDR). The PW package is only available left-end taped and reeled (e.g., TLV2332IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

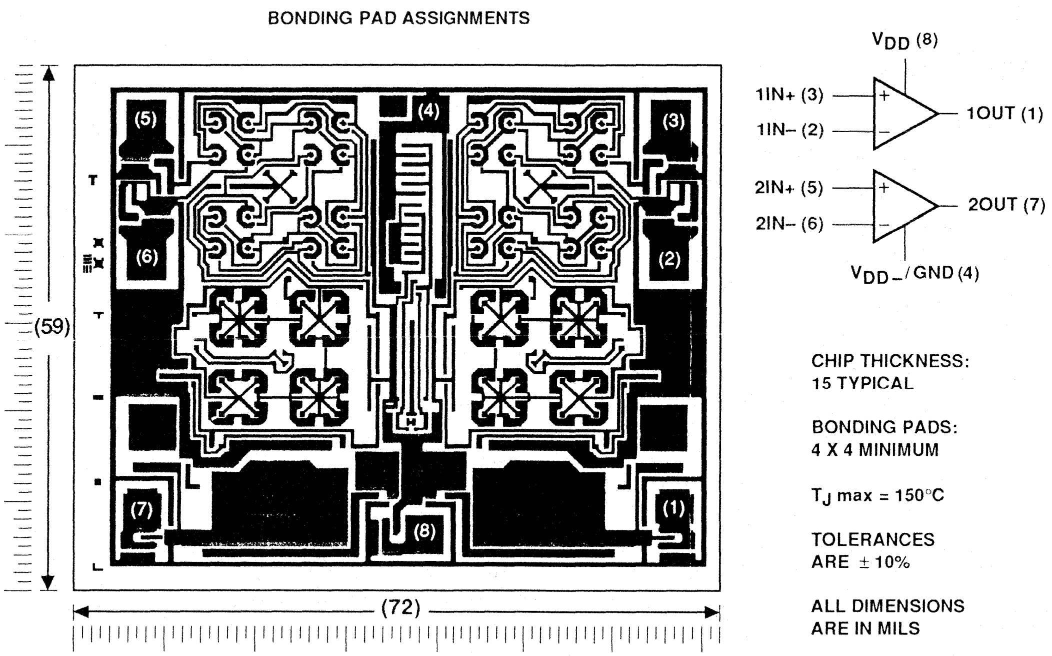
description (continued)

To facilitate the design of small portable equipment, the TLV2332 is made available in a wide range of package options, including the small-outline and thin-scaled-small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2332 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2332Y chip information

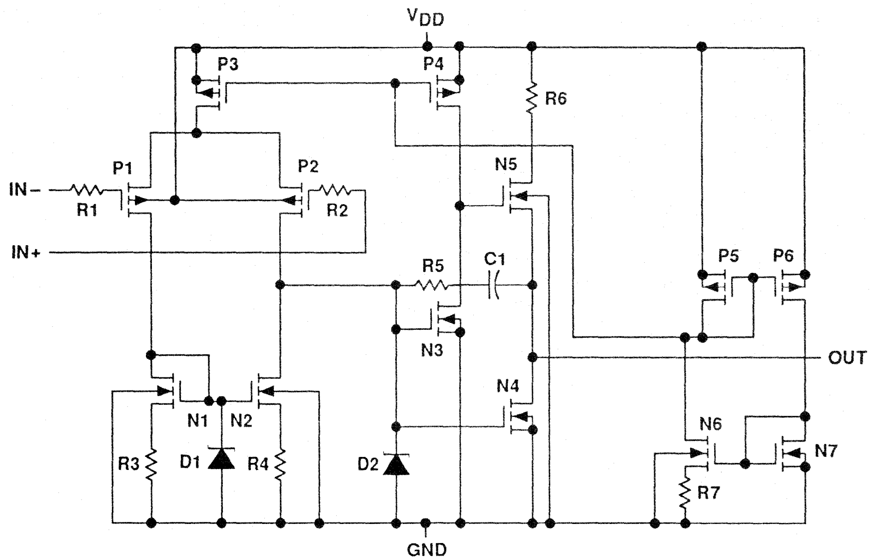
These chips, properly assembled, display characteristics similar to the TLV2332I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



equivalent schematic (each amplifier)

COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

†Includes both amplifiers and all ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . . . 8 V
Differential input voltage (see Note 2) . . . . . ± V_{DD}
Input voltage range, V_I (any input) . . . . . – 0.3 V to V_{DD}
Input current, I_I . . . . . ± 5 mA
Output current, I_O . . . . . ± 30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . – 40°C to 85°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package . . . . . 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	−0.2	1.8	V
	$V_{DD} = 5$ V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		µV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		160	500		210	560	µA
			Full range			620			800	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 30		25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 30		25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		−40°C		43°		
				25°C		40°		
				85°C		38°		

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ		0.6	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	94		70	94		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		160	500		210	560	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Gain-bandwidth product	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE

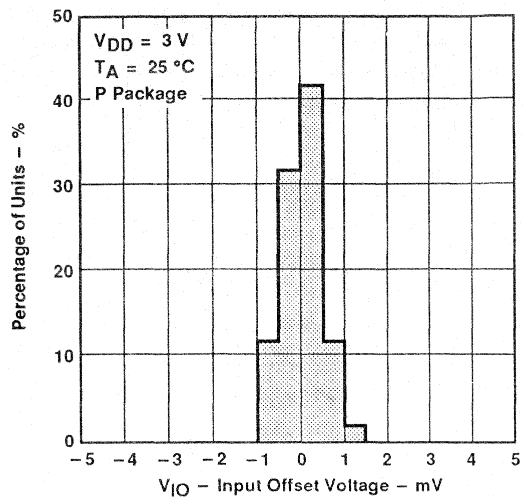


Figure 1

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE

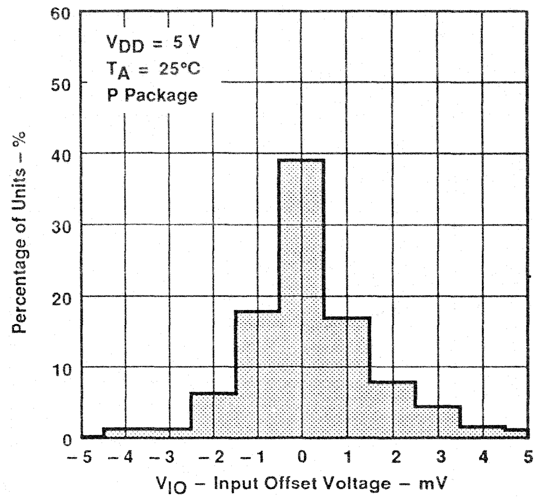


Figure 2

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

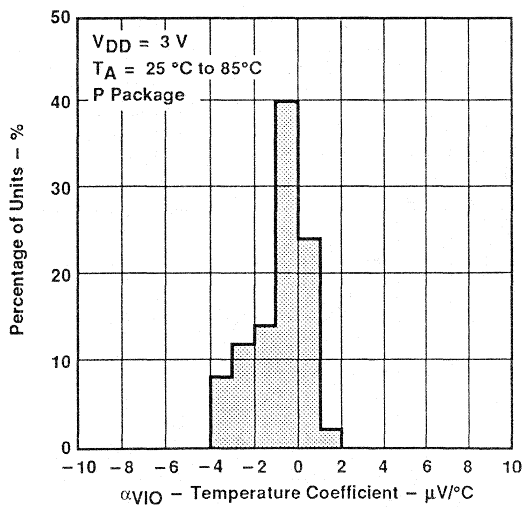


Figure 3

DISTRIBUTION OF TLV2332
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

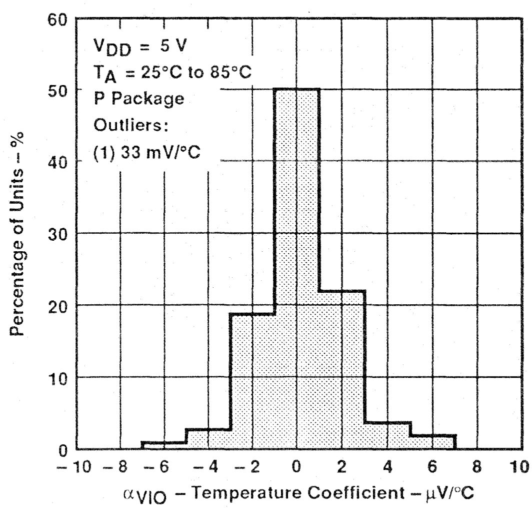


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

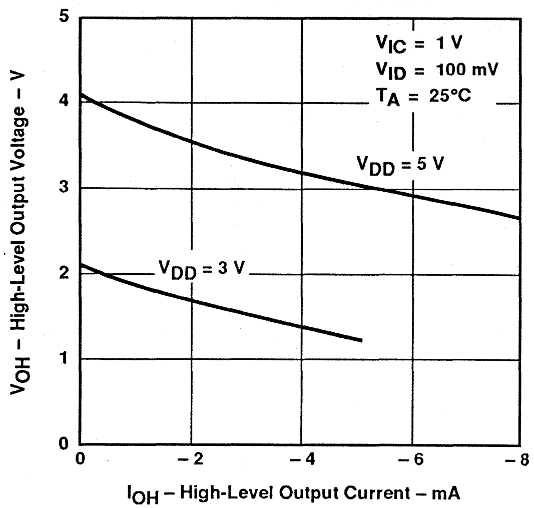


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

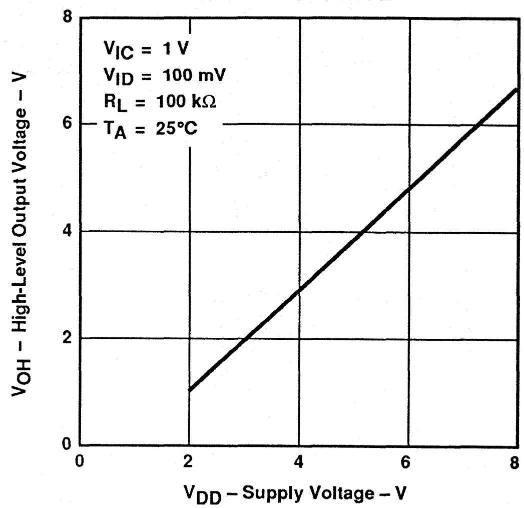


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

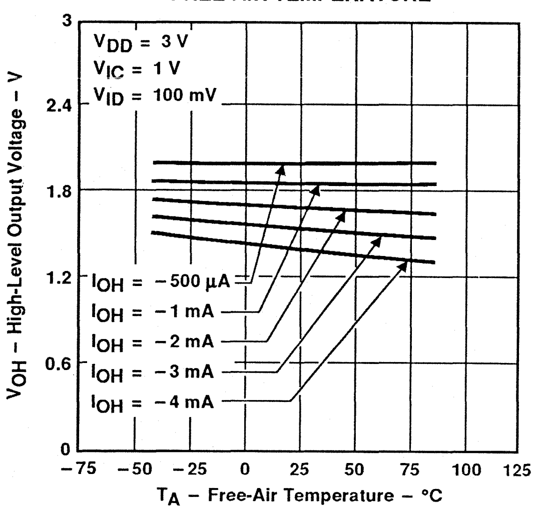


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

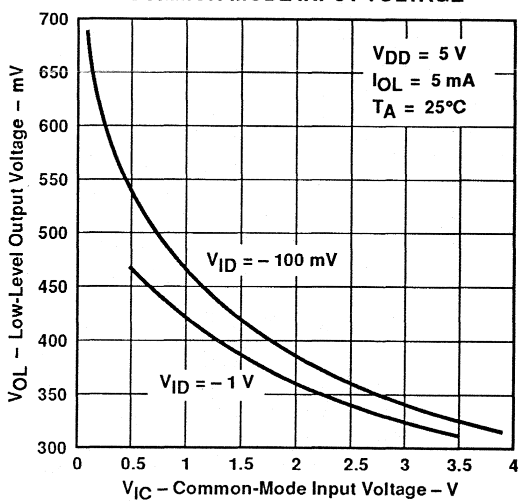


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

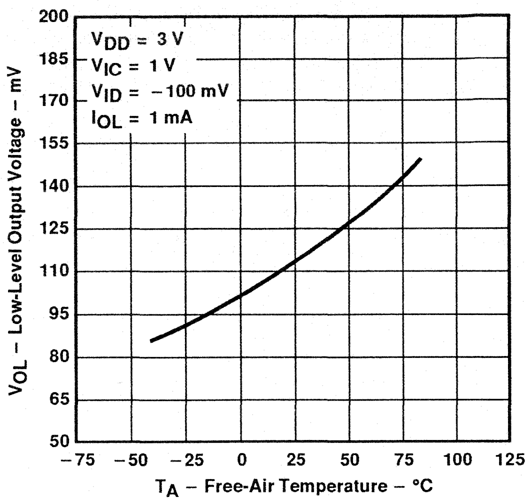


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

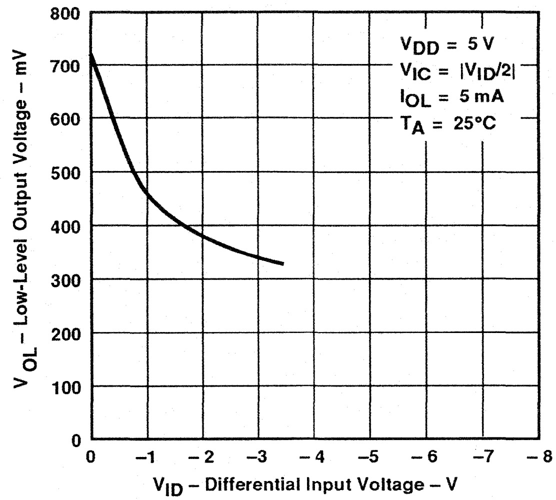


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

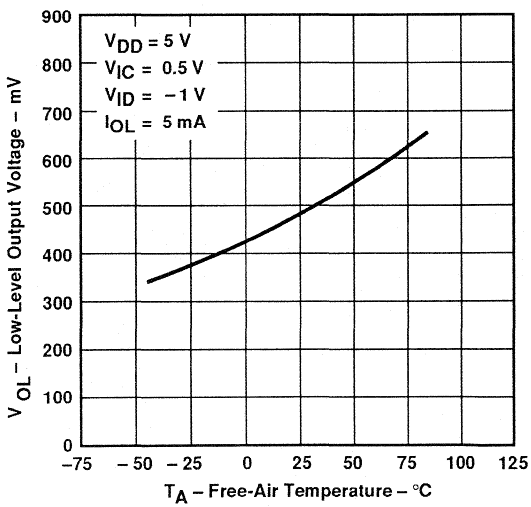


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

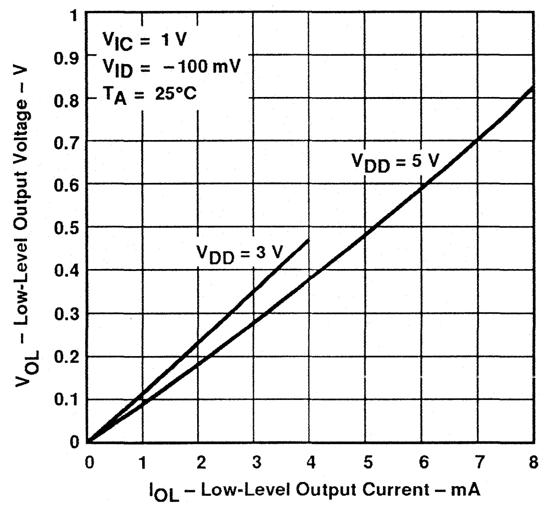


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

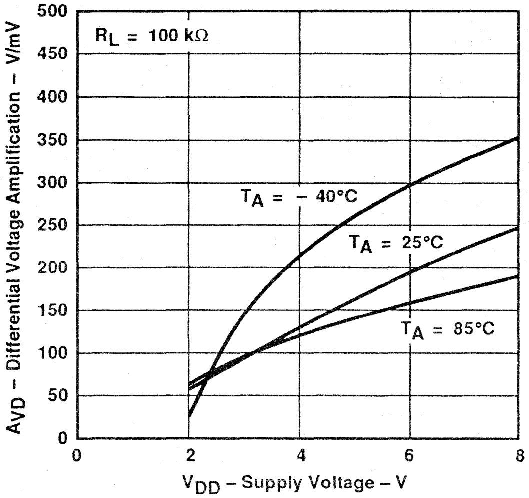


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

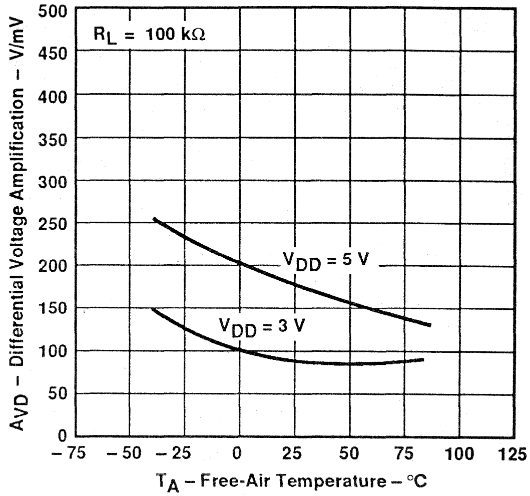


Figure 14

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

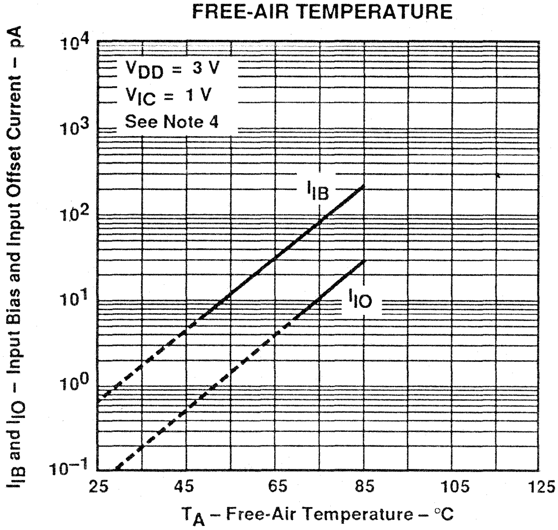


Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

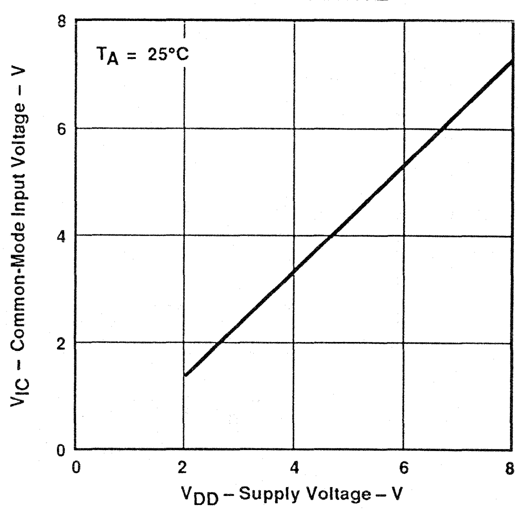


Figure 16

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

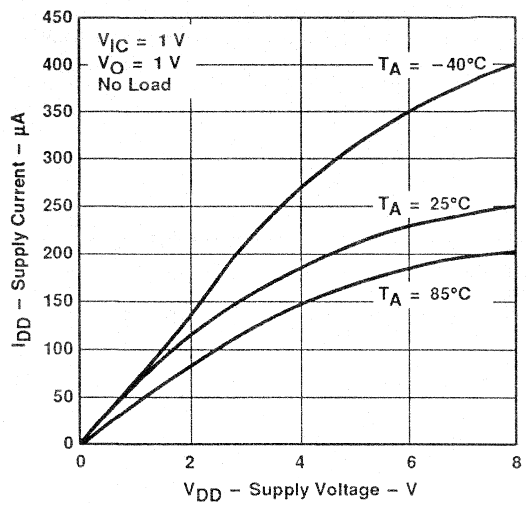


Figure 17

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

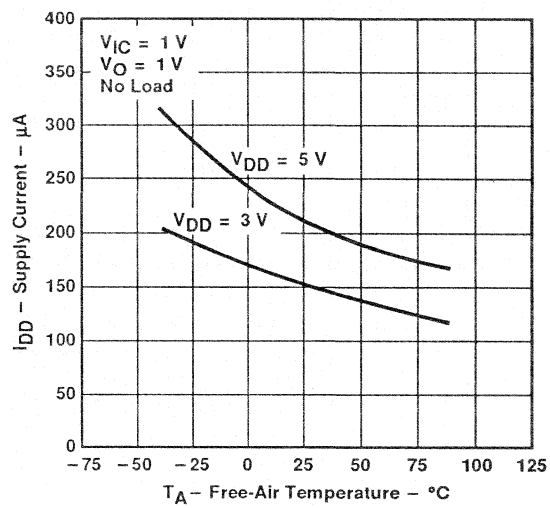


Figure 18

SLEW RATE
vs
SUPPLY VOLTAGE

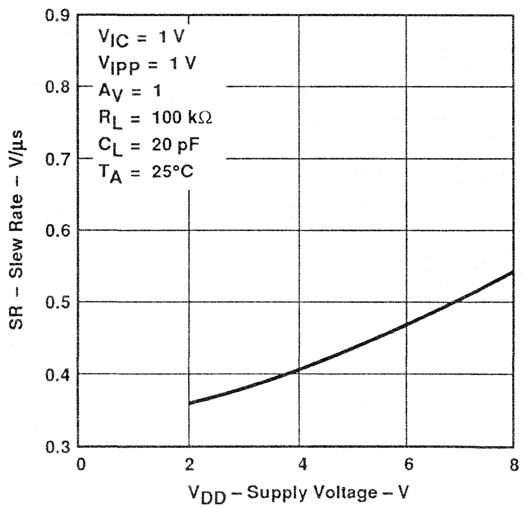


Figure 19

SLEW RATE
vs
FREE-AIR TEMPERATURE

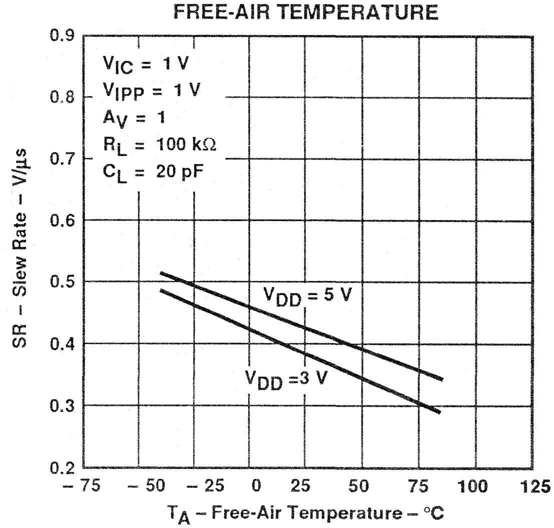


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

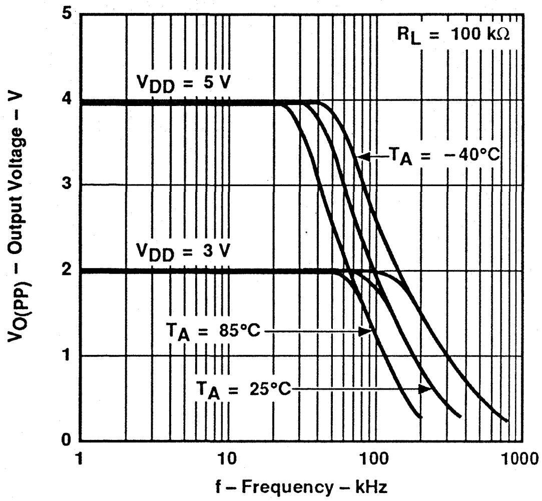


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

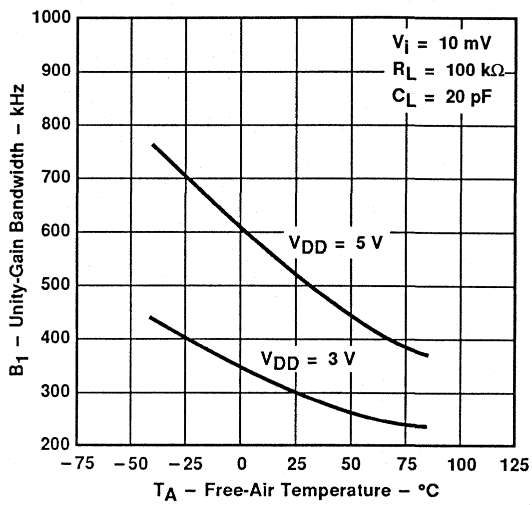


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

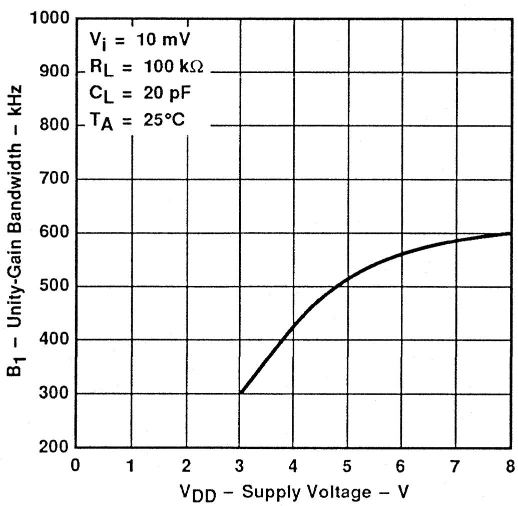


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

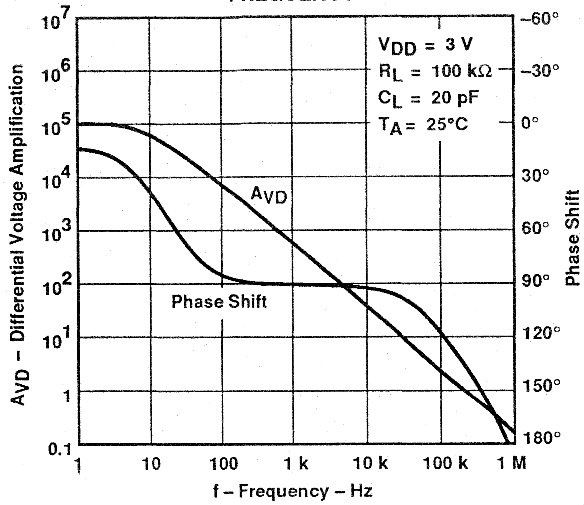


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

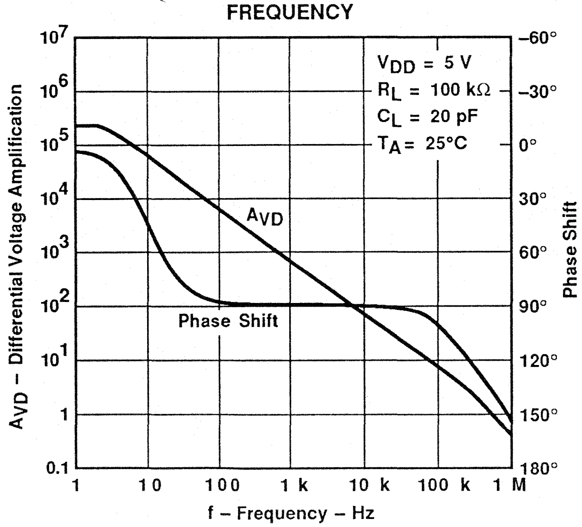


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

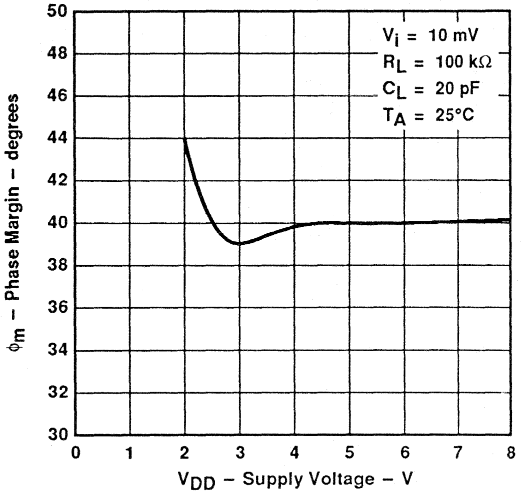


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

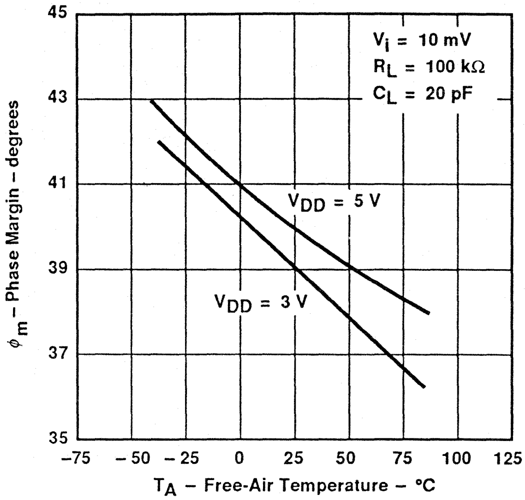


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

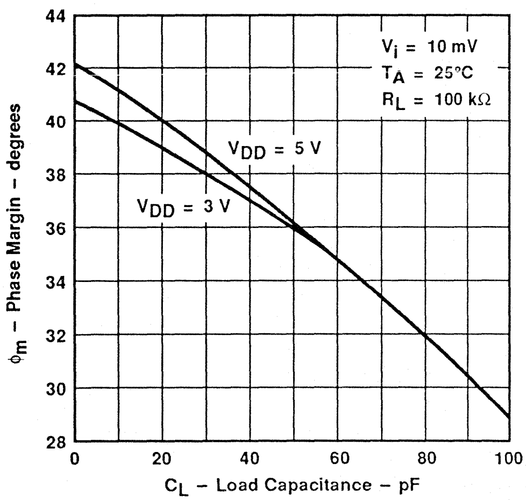


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

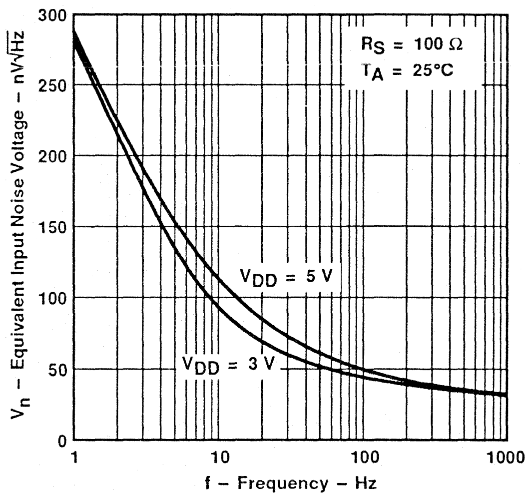
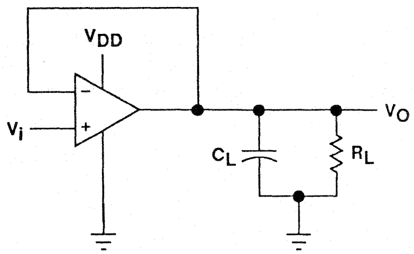


Figure 29

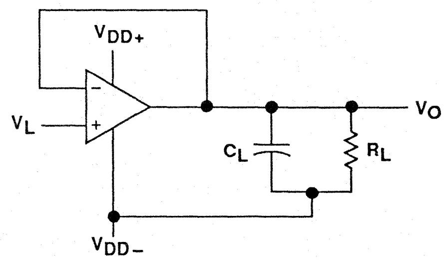
PARAMETER MEASUREMENT INFORMATION

single-supply versus split-supply test circuits

Because the TLV2332 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.

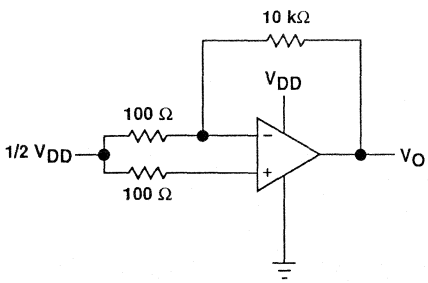


(a) SINGLE-SUPPLY

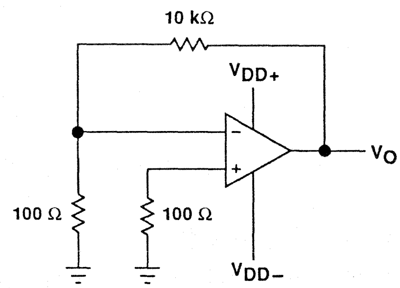


(b) SPLIT-SUPPLY

Figure 30. Unity-Gain Amplifier

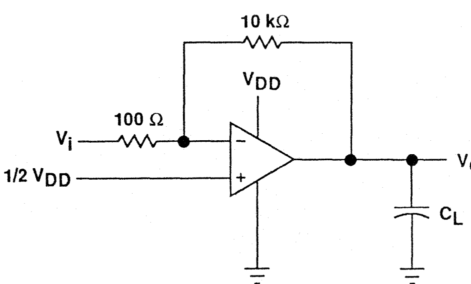


(a) SINGLE-SUPPLY

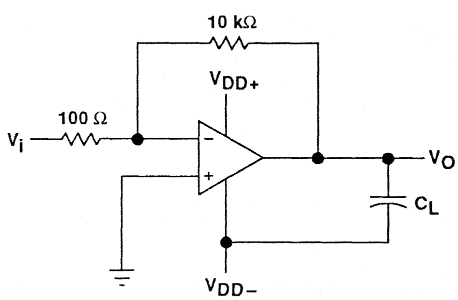


(b) SPLIT-SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE-SUPPLY



(b) SPLIT-SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2332 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

   One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

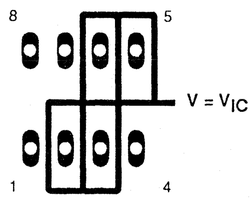


Figure 33. Isolation Metal Around Device Inputs
(P Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

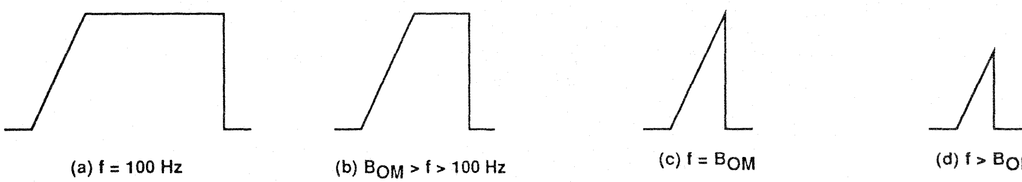


Figure 34. Full-Power-Response Output Signal

test time

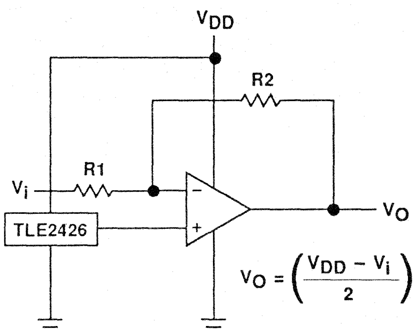
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLV2332 will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.



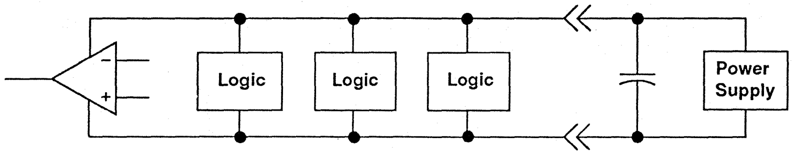
$$V_O = \left(\frac{V_{DD} - V_i}{2}\right)\frac{R_2}{R_1} + \frac{V_{DD}}{2}$$

Figure 35. Inverting Amplifier With Voltage Reference

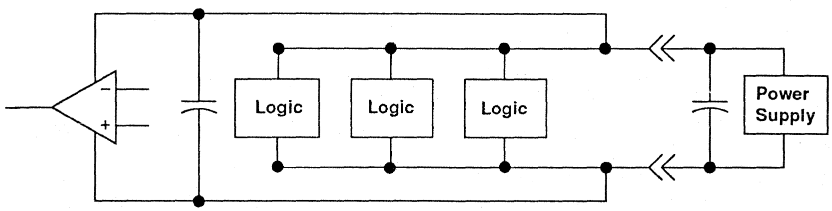
TYPICAL APPLICATION DATA

The TLV2332 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

Figure 36. Common Versus Separate Supply Rails

input characteristics

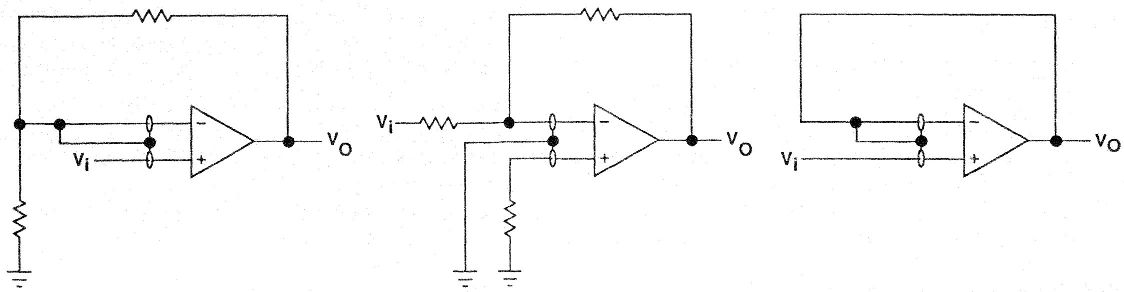
The TLV2332 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2332 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLV2332 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA



(a) NONINVERTING AMPLIFIER (b) INVERTING AMPLIFIER (c) UNITY-GAIN AMPLIFIER

Figure 37. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2332 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

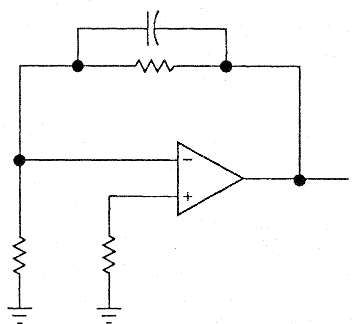


Figure 38. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2332 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2332 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

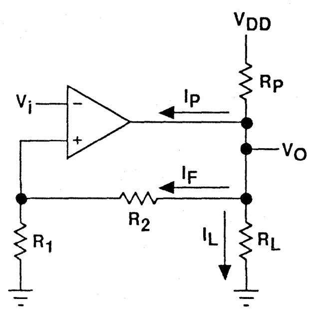
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2332 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2332 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2332 are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 41, 42, and 43). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 μA)

Figure 39. Resistive Pullup to Increase V_{OH}

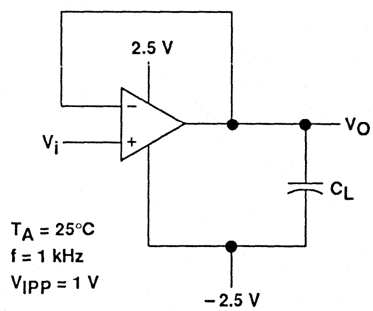
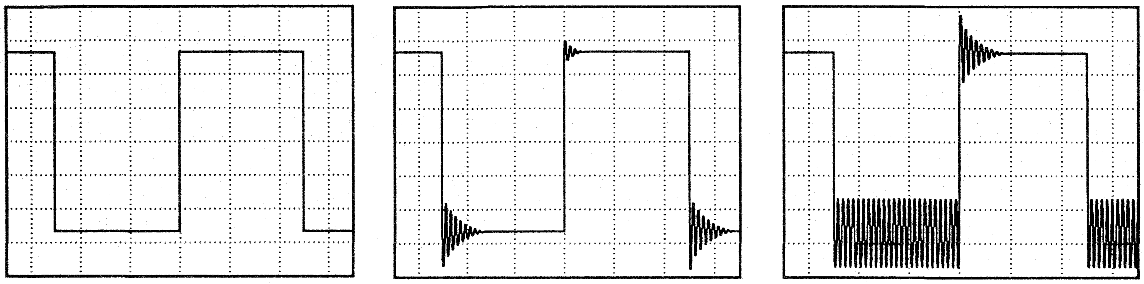


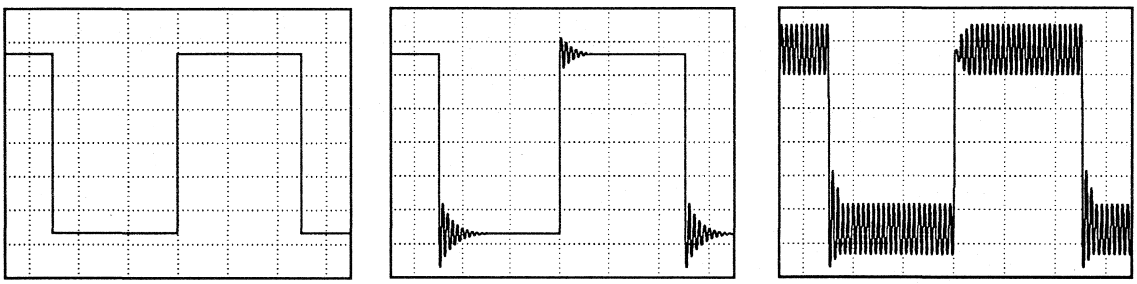
Figure 40. Test Circuit for Output Characteristics

TYPICAL APPLICATION DATA



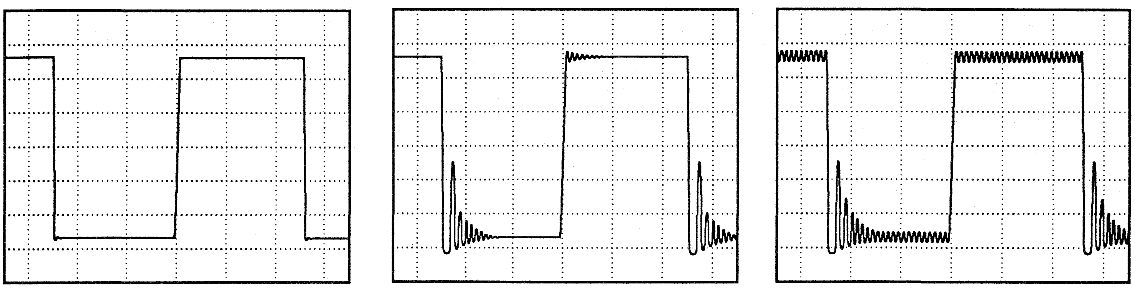
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 42. Effect of Capacitive Loads in Medium-Bias Mode

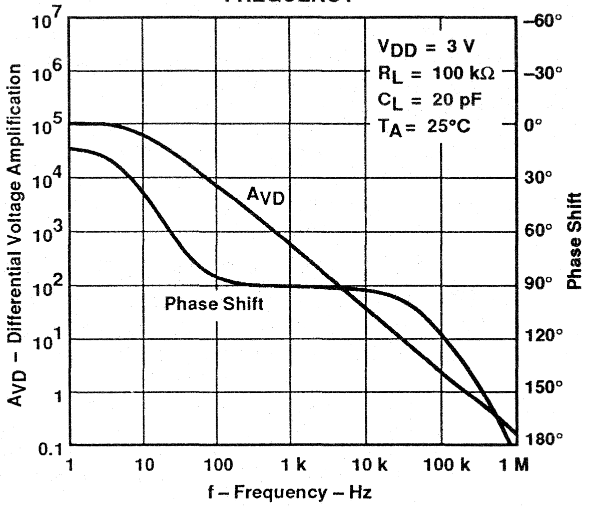


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 43. Effect of Capacitive Loads in Low-Bias Mode

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = – 40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} – 1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . $10^{12}\ \Omega$ Typical**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

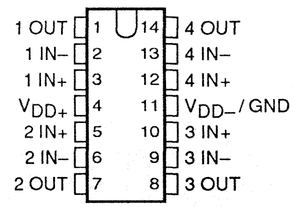


description

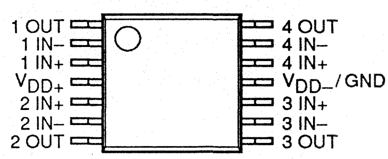
The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike the TLV2324 which is optimized for ultra-low power, the TLV2334 is designed to provide a combination of low power and good ac performance. Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V supplies over a temperature range of – 40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

Having a maximum supply current of only 300 µA per amplifier over the full temperature range, the TLV2334 devices offer a combination of good ac performance and microampere supply currents. From a 3-V power supply, the amplifiers typical slew rate is 0.38 V/µs, and its bandwidth is 300 kHz. These amplifiers offer a level of ac performance greater than that of many other devices operating at comparable power levels.

D OR N PACKAGE (TOP VIEW)



PW PACKAGE (TOP VIEW)



AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (N)	TSSOP (PW)	
– 40°C to 85°C	10 mV	TLV2334ID	TLV2334IN	TLV2334IPW	TLV2334Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2334IDR). The PW package is only available left-end taped and reeled (e.g., TLV2334IPWLE).

TEXAS INSTRUMENTS

description (continued)

The TLV2334 operational amplifiers are especially well suited for use in low-current or battery-powered applications.

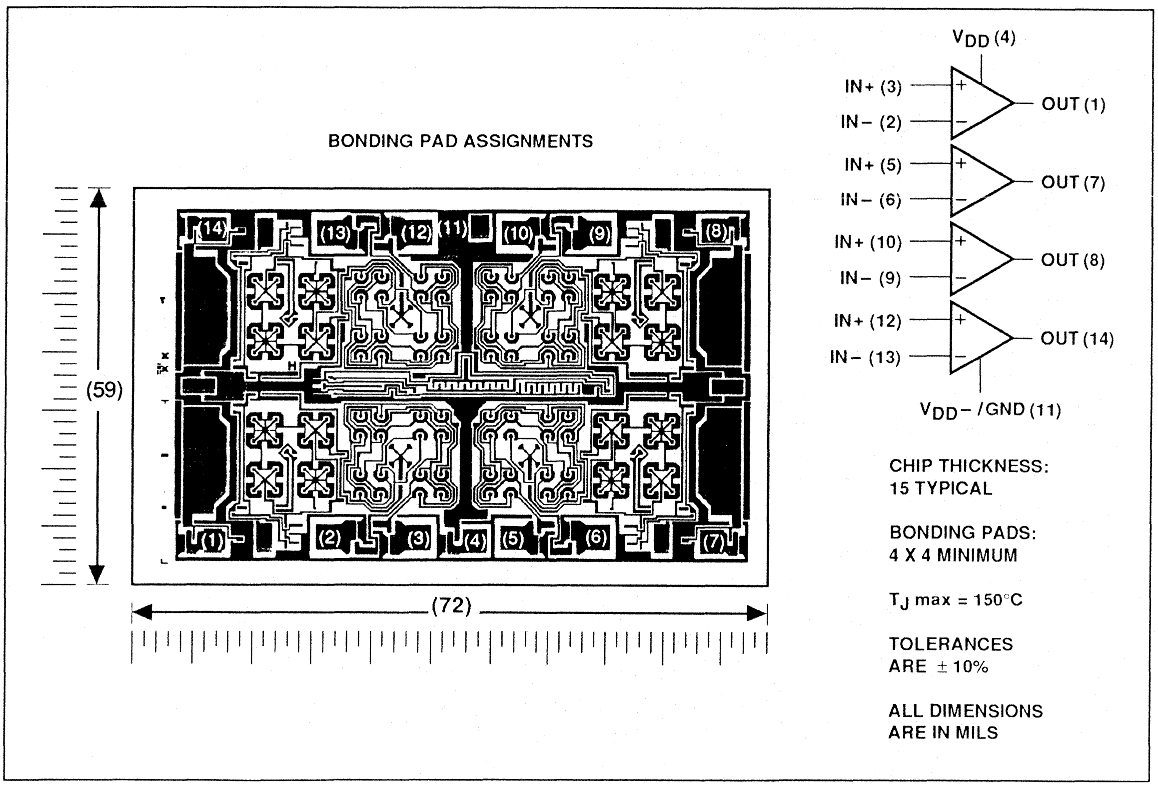
Low-voltage and low-power operation has been made possible by using Texas Instruments silicon gate LinCMOS technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents making them ideal for interfacing to high-impedance sources such as in sensor circuits or filter applications.

To facilitate the design of small portable equipment, the TLV2334 is made available in a wide range of package options, including the small-outline and thin-scaled-small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2334 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

TLV2334Y chip information

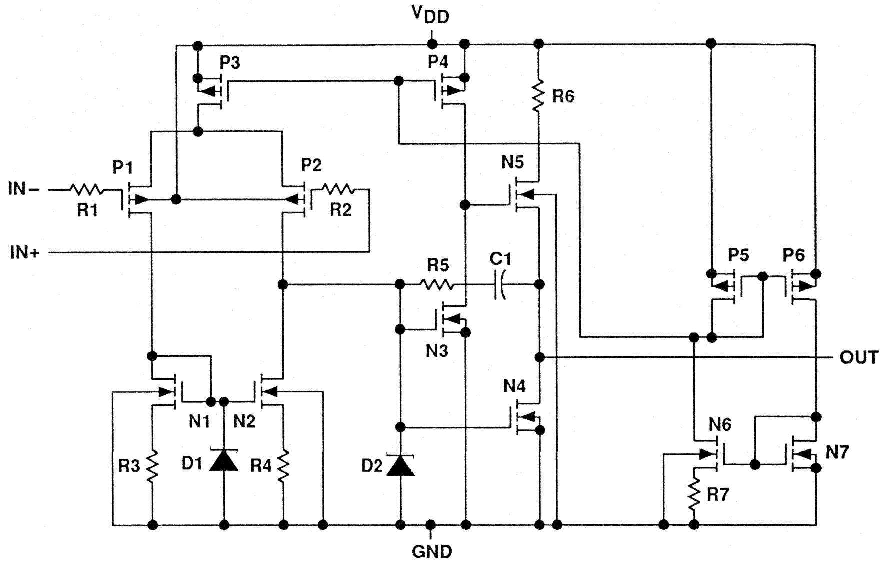
These chips, properly assembled, display characteristics similar to the TLV2334I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



equivalent schematic (each amplifier)

COMPONENT COUNT†	
Transistors	108
Diodes	8
Resistors	28
Capacitors	4

†Includes all amplifiers, ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) . . . 8 V
Differential input voltage (see Note 2) . . . ± V_{DD}
Input voltage range, V_I (any input) . . . – 0.3 V to V_{DD}
Input current, I_I . . . ± 5 mA
Output current, I_O . . . ± 30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . Unlimited
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . – 40°C to 85°C
Storage temperature range . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package . . . 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1575 mW	12.6 mW/°C	819 mW
PW	700 mW	5.6 mW/°C	364 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	−0.2	1.8	V
	$V_{DD} = 5$ V	−0.2	3.8	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V MIN	V_{DD} = 3 V TYP	V_{DD} = 3 V MAX	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		320	1000		420	1120	μA
			Full range			1200			1600	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 30		25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 100 kΩ, See Figure 30		25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 100 kΩ, See Figure 32		−40°C		43°		
				25°C		40°		
				85°C		38°		

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ		0.6	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	94		70	94		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		320	1000		420	1120	µA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Gain-bandwidth product	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE

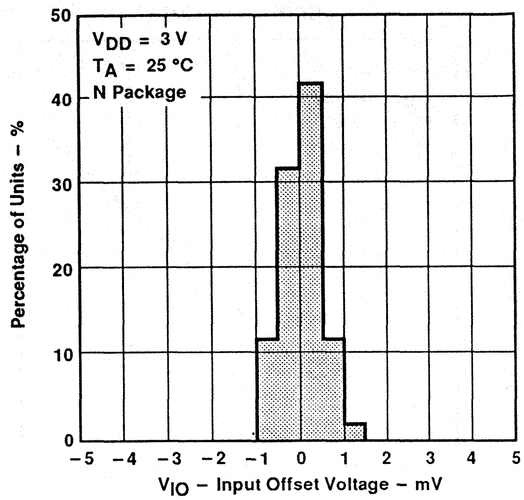


Figure 1

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE

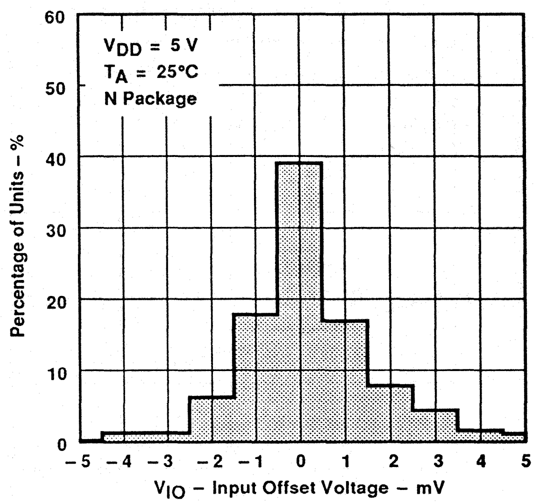


Figure 2

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

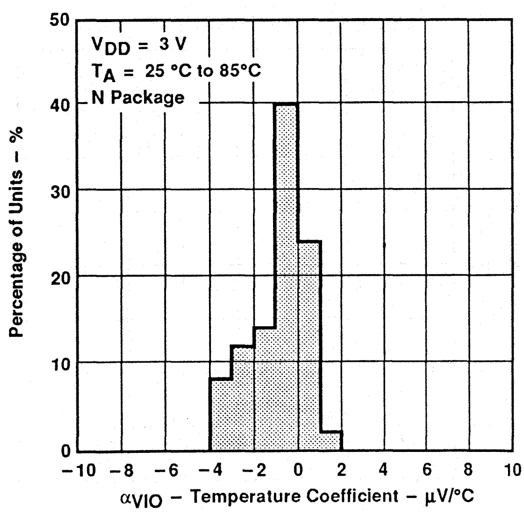


Figure 3

DISTRIBUTION OF TLV2334
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

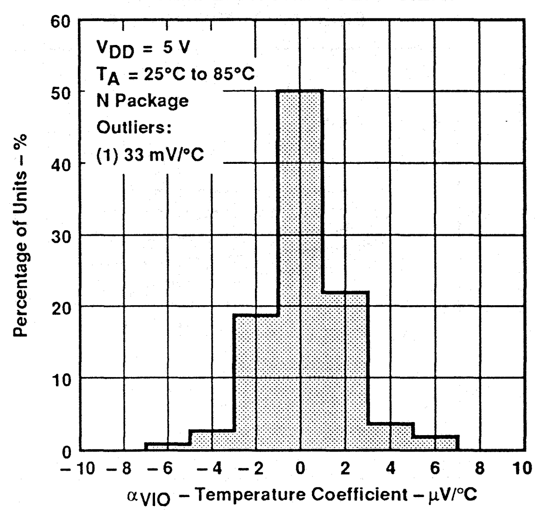


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

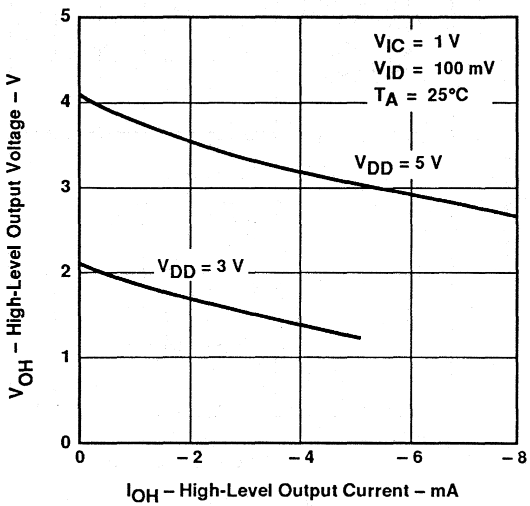


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

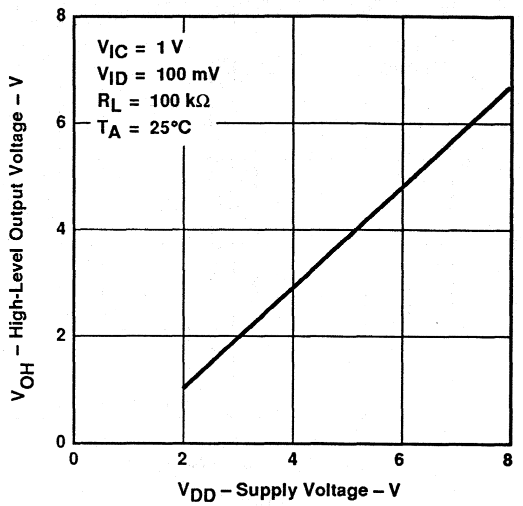


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

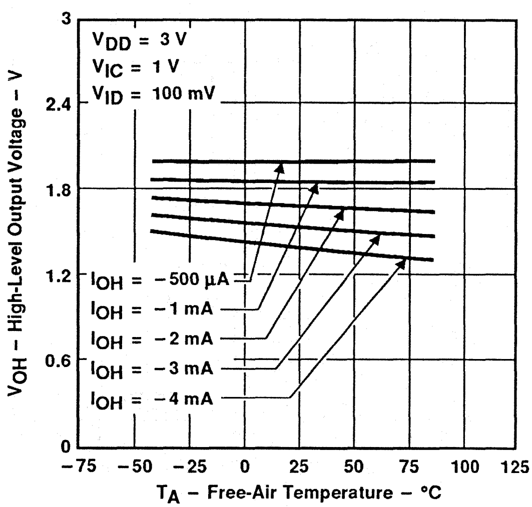


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

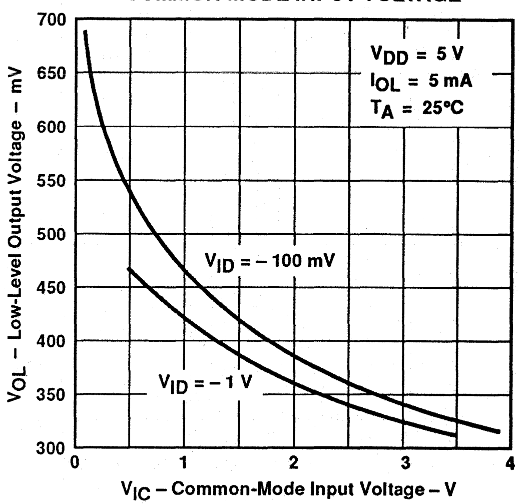


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

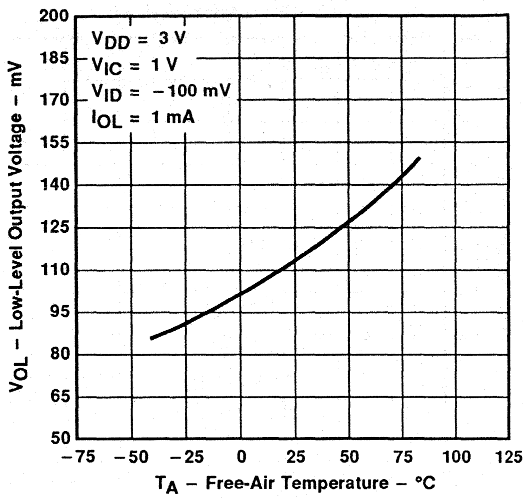


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

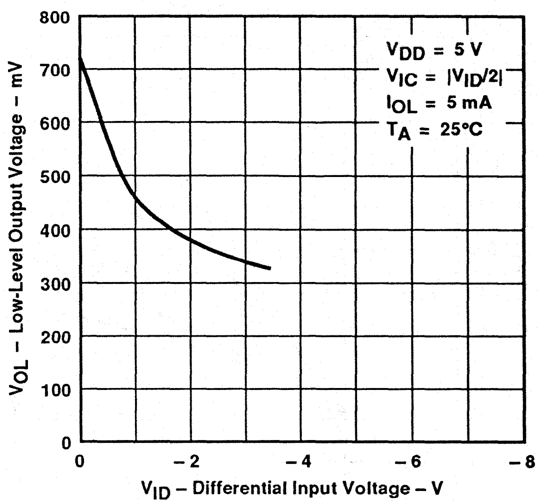


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

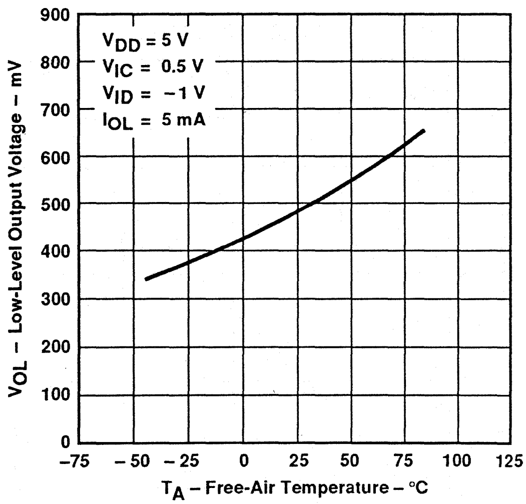


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

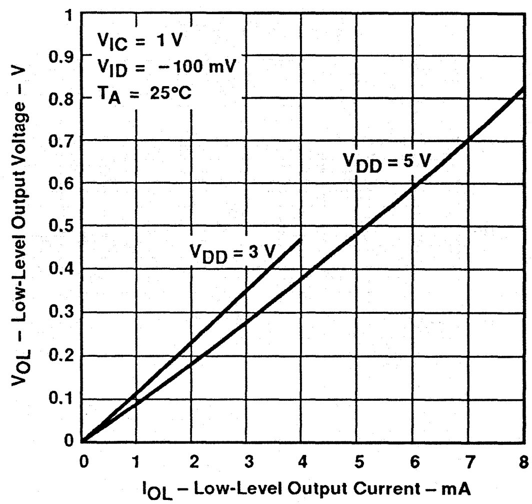


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

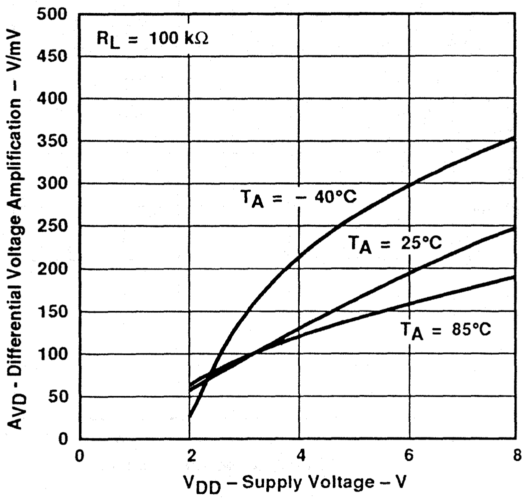


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

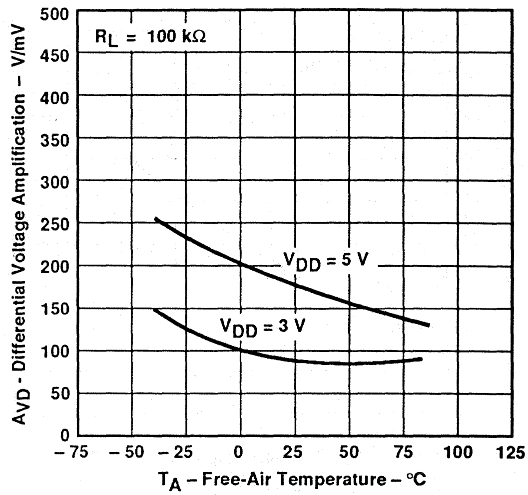


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

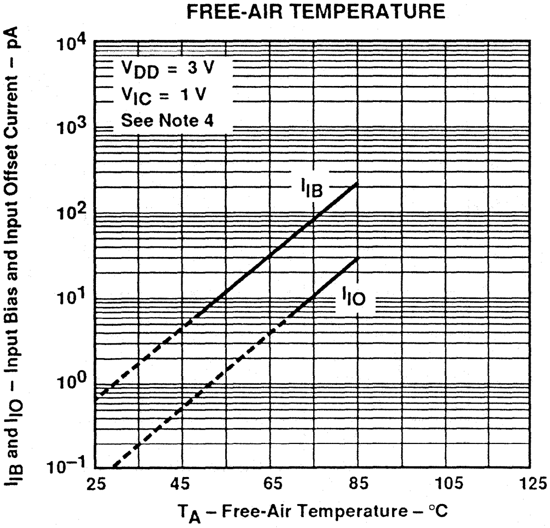


Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

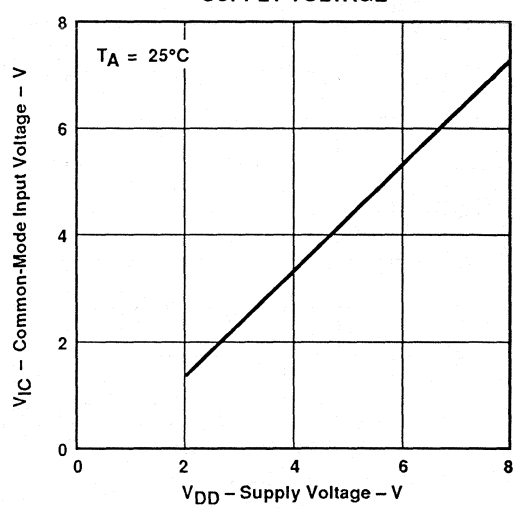


Figure 16

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

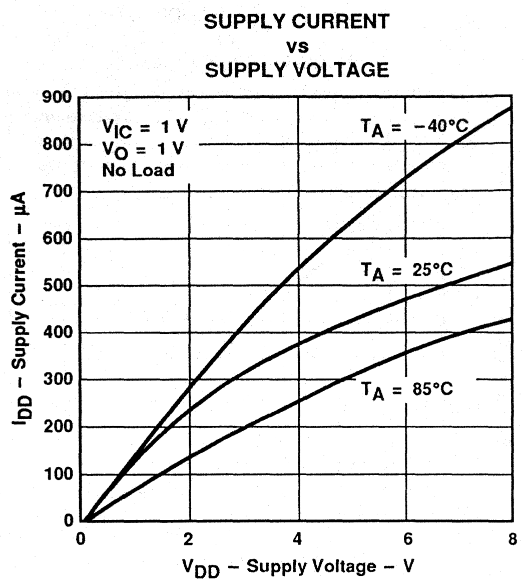


Figure 17

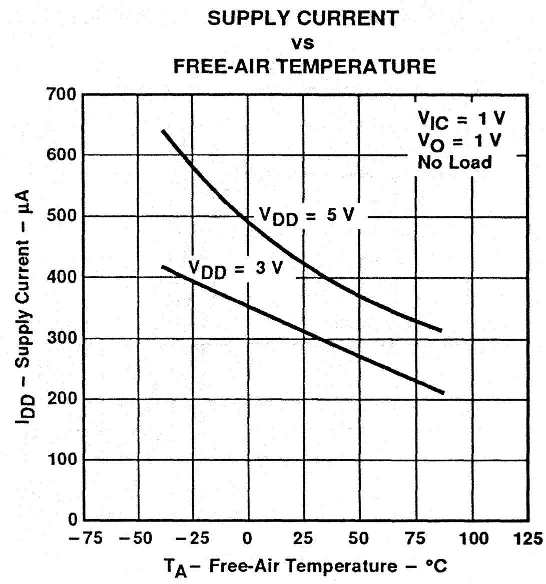


Figure 18

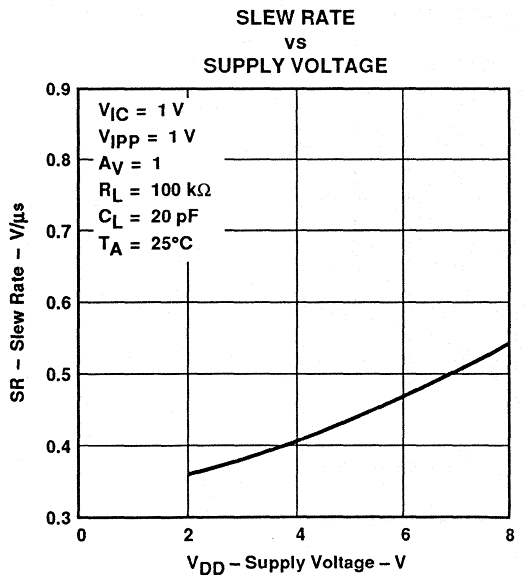


Figure 19

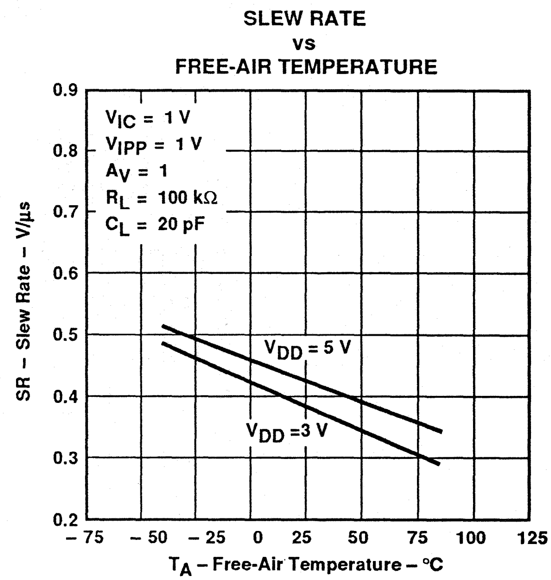


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

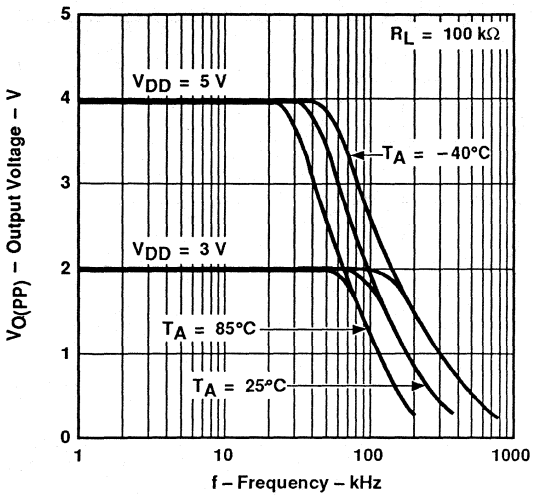


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

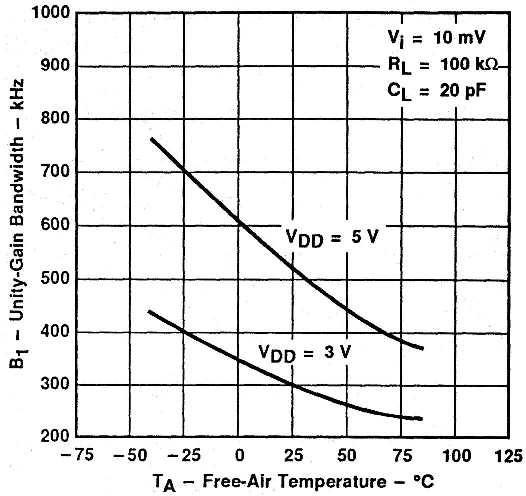


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

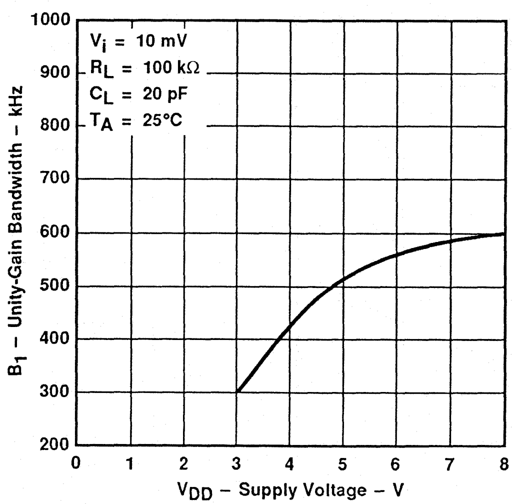


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

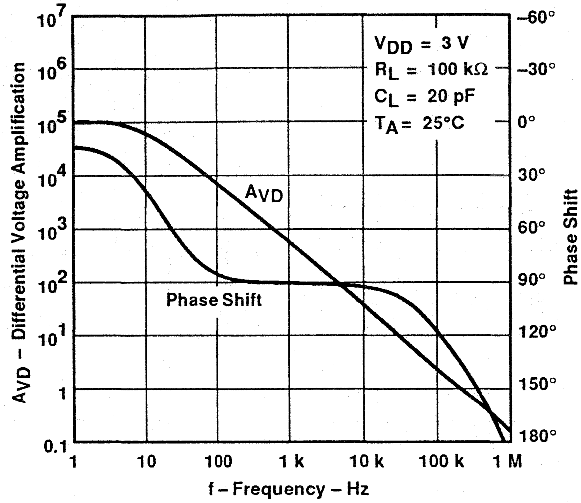


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

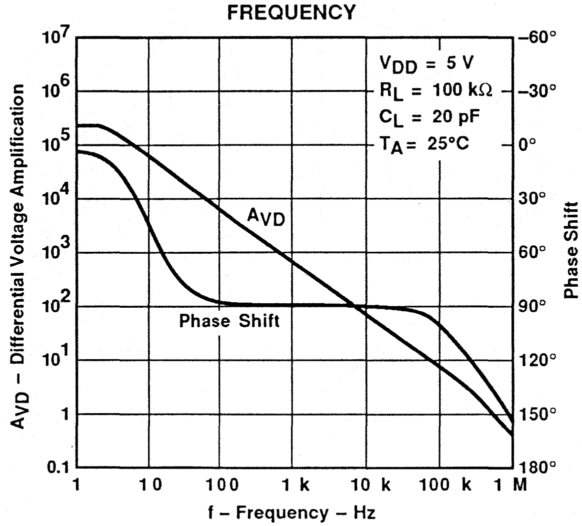


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN
vs
SUPPLY VOLTAGE

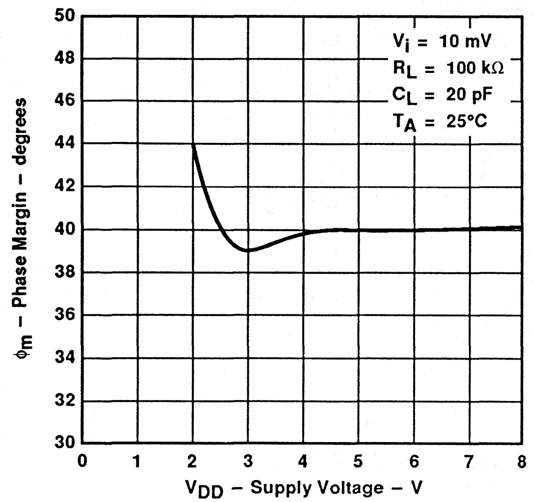


Figure 26

PHASE MARGIN
vs
FREE-AIR TEMPERATURE

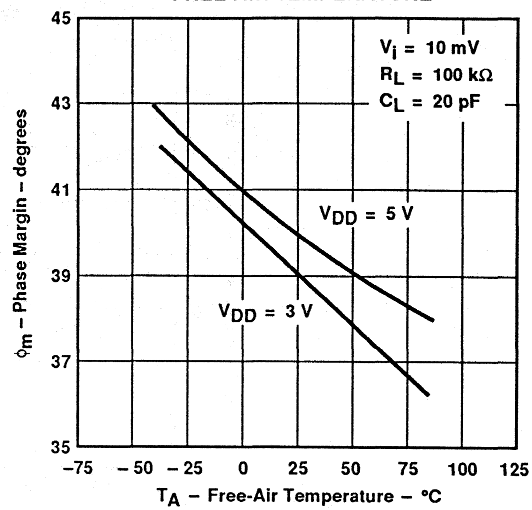


Figure 27

PHASE MARGIN
vs
LOAD CAPACITANCE

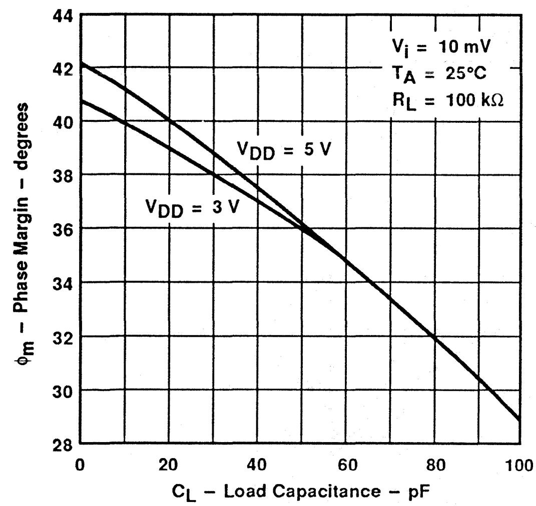


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

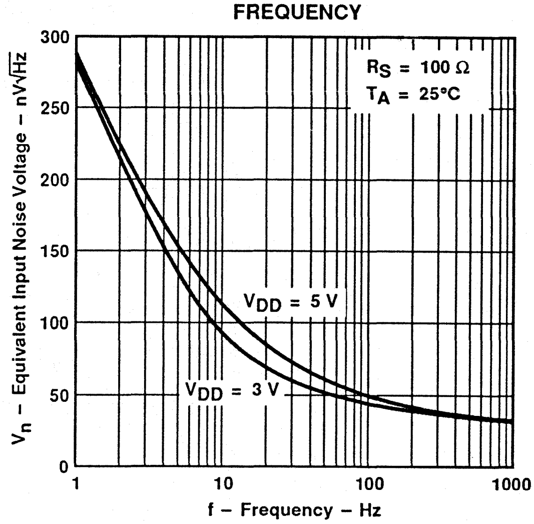
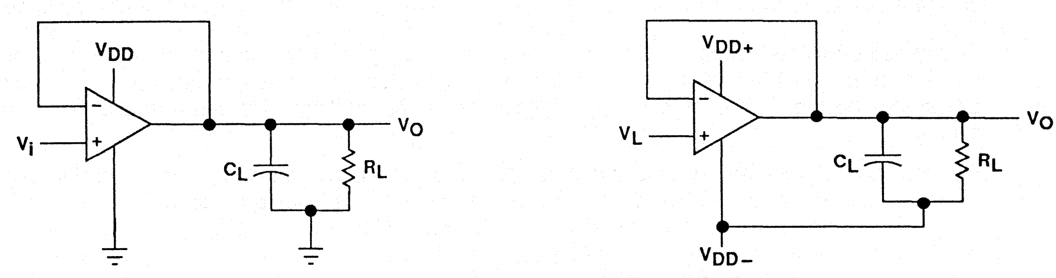


Figure 29

PARAMETER MEASUREMENT INFORMATION

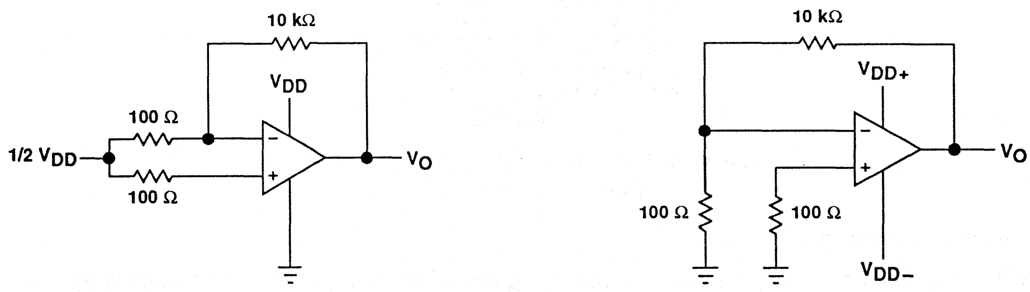
single-supply versus split-supply test circuits

Because the TLV2334I is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



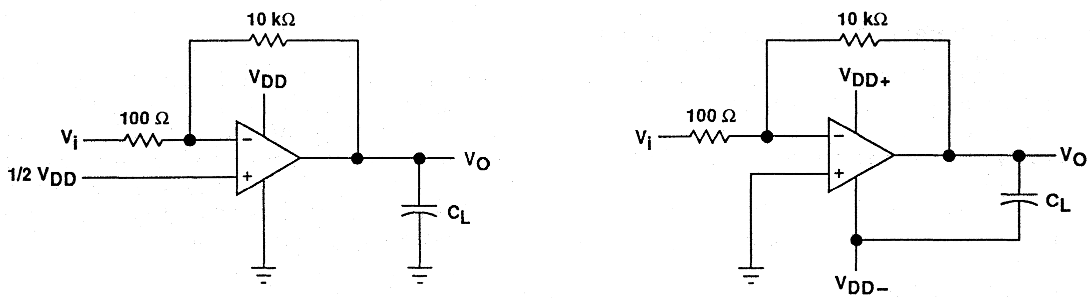
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2334I operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

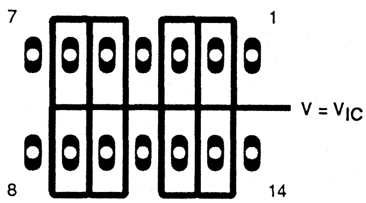


Figure 33. Isolation Metal Around Device Inputs (N Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

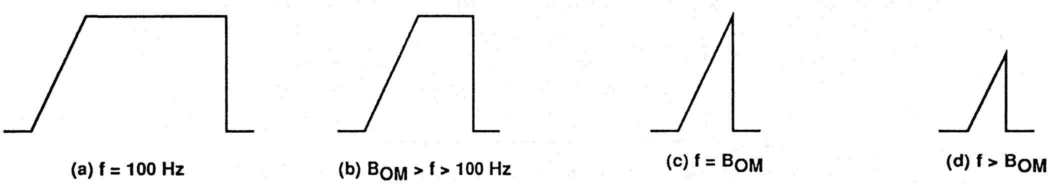


Figure 34. Full-Power-Response Output Signal

test time

Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLV2334I will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.

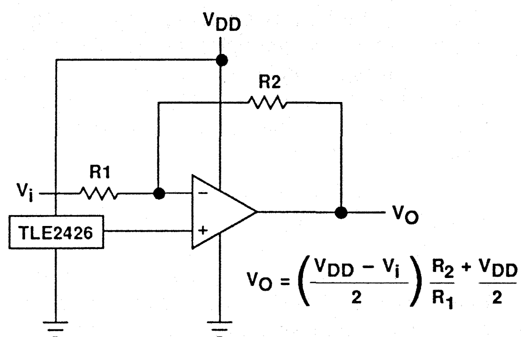
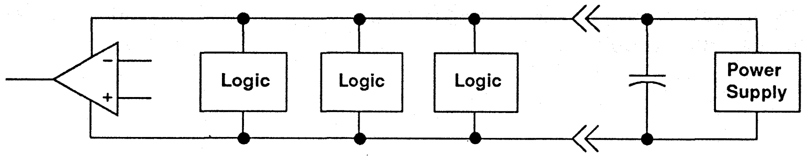


Figure 35. Inverting Amplifier With Voltage Reference

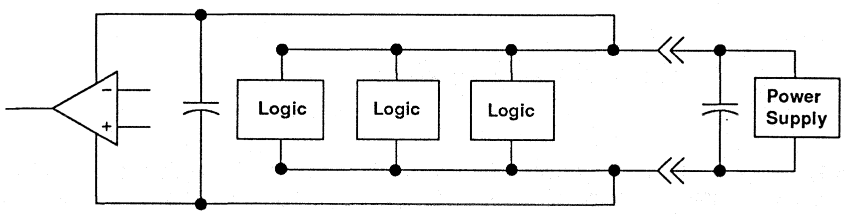
TYPICAL APPLICATION DATA

The TLV2334I works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2334I is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2334I very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLV2334I is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

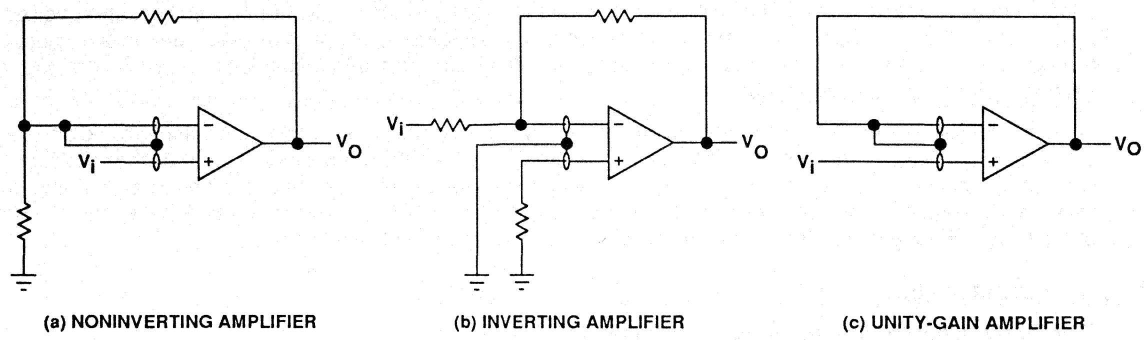


Figure 37. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2334I results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

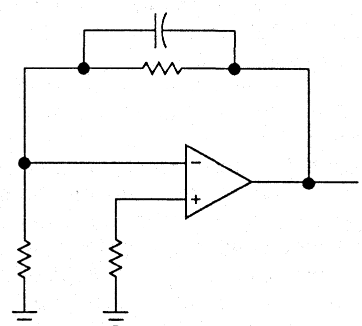


Figure 38. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2334I incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2334I inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2334I is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2334I possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2334I are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 41, 42, and 43). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

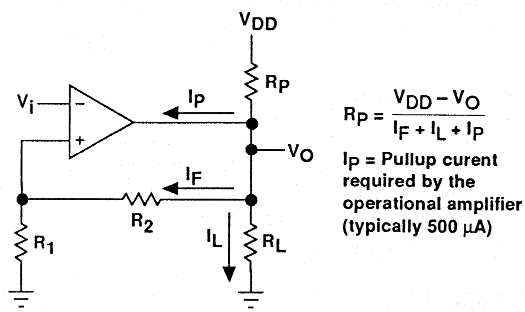


Figure 39. Resistive Pullup to Increase V_{OH}

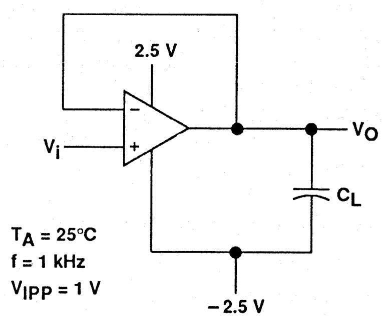
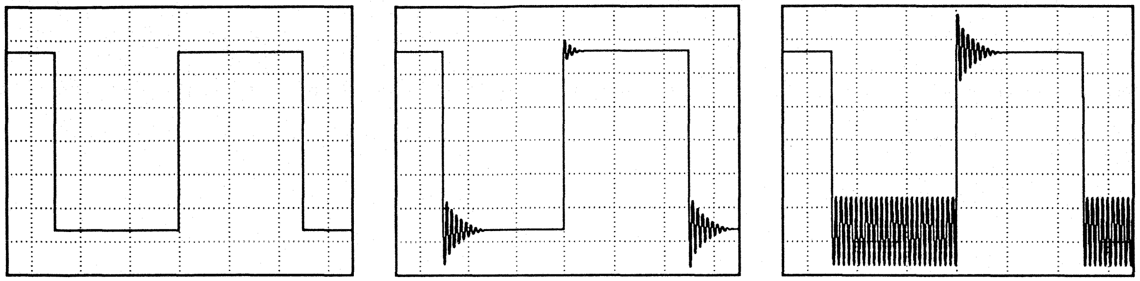


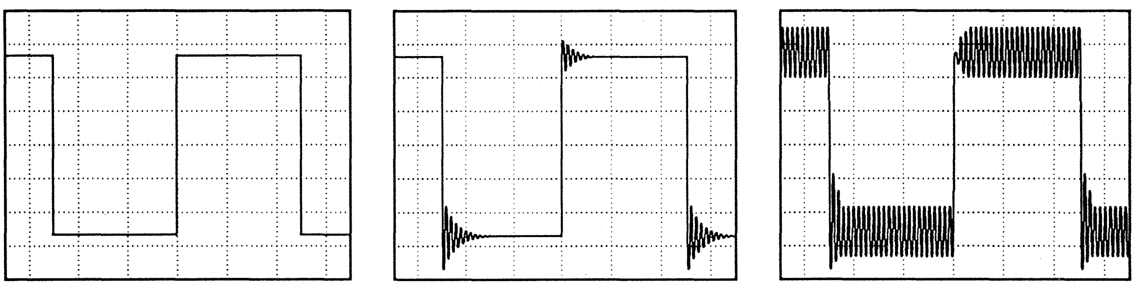
Figure 40. Test Circuit for OutputCharacteristics

TYPICAL APPLICATION DATA



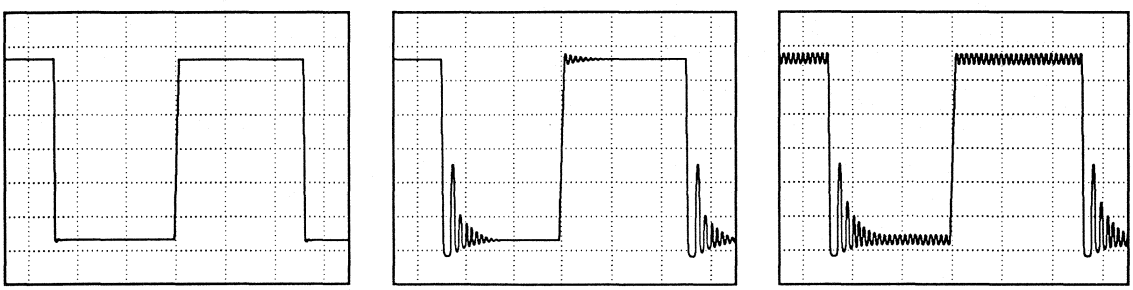
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 42. Effect of Capacitive Loads in Medium-Bias Mode



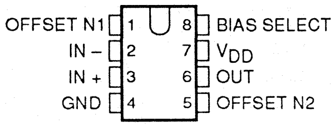
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 43. Effect of Capacitive Loads in Low-Bias Mode

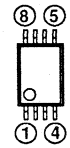
SLOS110–D4018, MAY 1992

- **Wide Range of Supply Voltages Over Specified Temperature Range: T_A = − 40°C to 85°C . . . 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Single-Supply Operation**
- **Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} − 1 V at 25°C**
- **Output Voltage Range Includes Negative Rail**
- **High Input Impedance . . . 10^{12} Ω Typical**
- **Low Noise . . . 25 nV/√Hz Typically at f = 1 kHz (High-Bias Mode)**
- **ESD-Protection Circuitry**
- **Designed-In Latch-Up Immunity**
- **Bias-Select Feature Enables Maximum Supply Current Range From 17 µA to 1.5 mA at 25°C**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



description

The TLV2341 operational amplifier has been specifically developed for low-voltage, single-supply applications and is fully specified to operate over a voltage range of 2 V to 8 V. The device uses the Texas Instruments silicon-gate LinCMOS™ technology to facilitate low-power, low-voltage operation and excellent offset-voltage stability. LinCMOS™ technology also enables extremely high input impedance and low bias currents allowing direct interface to high-impedance sources.

The TLV2341 offers a bias-select feature, which allows the device to effectively be programmed with a wide range of different supply currents, and therefore different levels of ac performance. The supply current can be set at 17 µA, 250 µA, or 1.5 mA, which results in a slew-rate specifications between 0.02 and 2.1 V/µs (at 3 V).

The TLV2341 operational amplifiers are especially well suited to single-supply applications and are fully specified and characterized at 3-V and 5-V power supplies. This low-voltage single-supply operation combined with low power consumption makes this device a good choice for remote, inaccessible, or portable battery-powered applications. The common-mode input range includes the negative rail.

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
− 40°C to 85°C	8 mV	TLV2341ID	TLV2341IP	TLV2341IPW	TLV2341Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2341IDR). The PW package is only available left-end taped and reeled (e.g., TLV2341IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

description (continued)

The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up.

The TLV2341 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD 883 C, Methods 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parameric performance.

bias-select feature

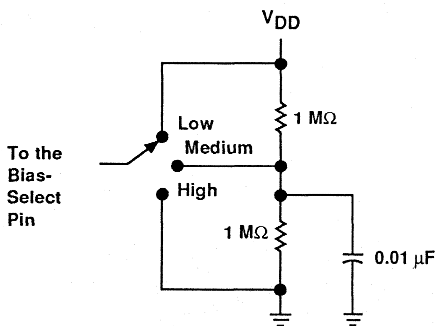
The TLV2341 offers a bias-select feature that allows the user to select any one of three bias levels, depending on the level of performance desired. The tradeoffs between bias levels involve ac performance and power dissipation (see Table 1).

Table 1. Effect of Bias Selection on Performance

TYPICAL PARAMETER VALUES $T_A = 25°C$, $V_{DD} = 3$ V		MODE			UNIT
		HIGH-BIAS $R_L = 10$ kΩ	MEDIUM-BIAS $R_L = 100$ kΩ	LOW-BIAS $R_L = 1$ MΩ	
P_D	Power dissipation	975	195	15	µW
SR	Slew rate	2.1	0.38	0.02	V/µs
V_n	Equivalent input noise voltage at f = 1 kHz	25	32	68	nV/√Hz
B_1	Unity-gain bandwidth	790	300	27	kHz
ϕ_m	Phase margin	49°	39°	34°	
A_{VD}	Large-signal differential voltage amplification	11	83	400	V/mV

bias selection

Bias selection is achieved by connecting the bias-select pin to one of three voltage levels (see Figure 1). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This procedure is simple in split-supply applications since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated in Figure 1. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS-SELECT VOLTAGE (Single Supply)
Low	V_{DD}
Medium	1 V to V_{DD} – 1 V
High	GND

Figure 1. Bias Selection for Single-Supply Applications

high-bias mode

In the high-bias mode, the TLV2341 series features low offset voltage drift, high input impedance, and low noise. Speed in this mode approaches that of BiFET devices but at only a fraction of the power dissipation.

medium-bias mode

The TLV2341 in the medium-bias mode features low offset voltage drift, high input impedance, and low noise. Speed in this mode is similar to general-purpose bipolar devices, but power dissipation is only a fraction of that consumed by bipolar devices.

low-bias mode

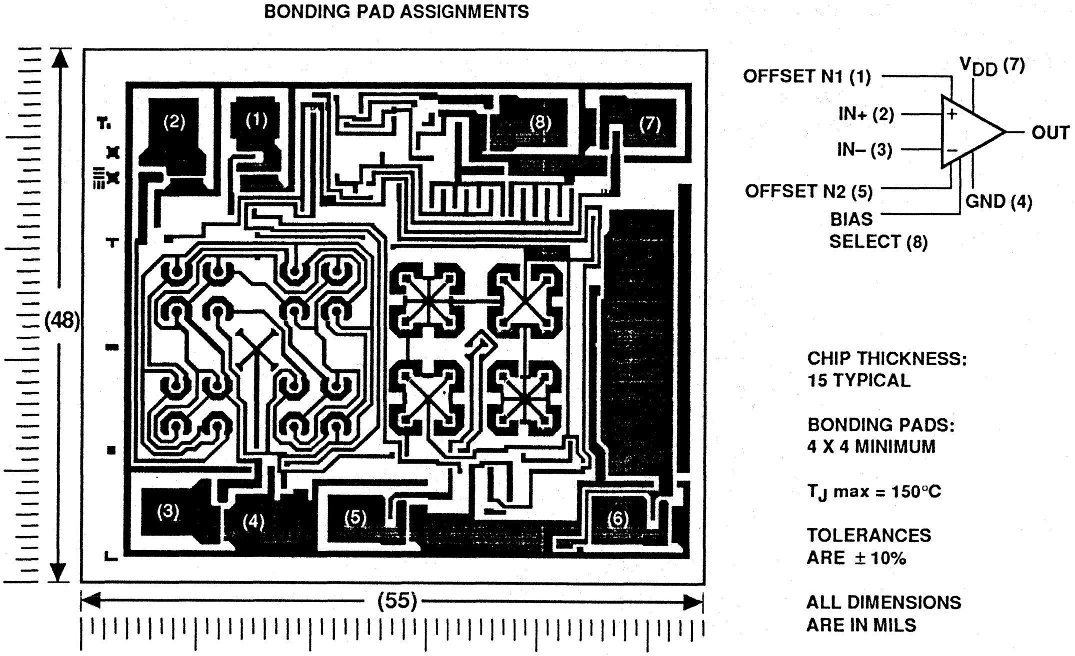
In the low-bias mode, the TLV2341 features low offset voltage drift, high input impedance, extremely low power consumption, and high differential voltage gain.

ORDER OF CONTENTS

TOPIC	BIAS MODE
schematic	all
absolute maximum ratings	all
recommended operating conditions	all
electrical characteristics operating characteristics typical characteristics	high (Figures 2 – 31)
electrical characteristics operating characteristics typical characteristics	medium (Figures 32 – 61)
electrical characteristics operating characteristics typical characteristics	low (Figures 62 – 91)
parameter measurement information	all
application information	all

TLV2341Y chip information

These chips, properly assembled, display characteristics similar to the TLV2341I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.



CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

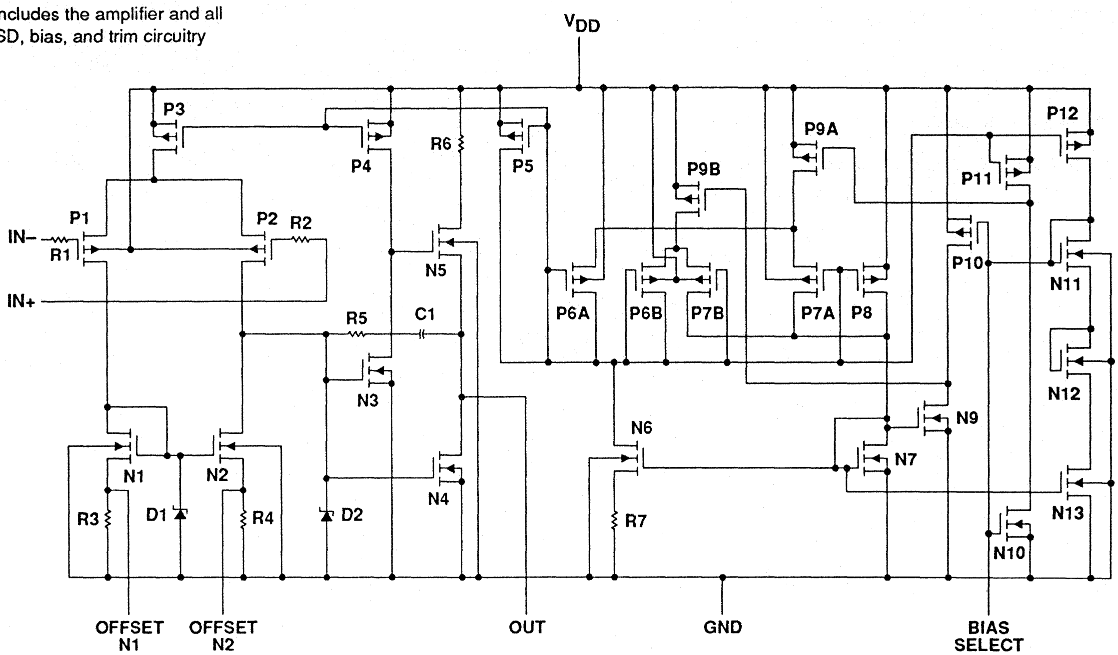
TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic

COMPONENT COUNT†	
Transistors	27
Diodes	2
Resistors	7
Capacitors	1

†Includes the amplifier and all ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) .... 8 V
Differential input voltage (see Note 2) .... $\pm V_{DD}$
Input voltage range, V_I (any input) .... – 0.3 V to V_{DD}
Input current, I_I .... ± 5 mA
Output current, I_O .... ± 30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) .... Unlimited
Continuous total dissipation .... See Dissipation Rating Table
Operating free-air temperature range, T_A .... – 40°C to 85°C
Storage temperature range .... – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package .... 260°C

†Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	–0.2	1.8	V
	$V_{DD} = 5$ V	–0.2	3.8	
Operating free-air temperature, T_A		–40	85	°C

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V MIN	TYP	MAX	V_{DD} = 5 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	− 0.2 to 2	− 0.3 to 2.3		− 0.2 to 4	− 0.3 to 4.2		V
			Full range	− 0.2 to 1.8			− 0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		− 1.2			− 1.4		μA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		325	1500		675	1600	μA
			Full range			2000			2200	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

HIGH-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 92	V_{IPP} = 1 V	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 93		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 92		25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 10 kΩ, See Figure 94		25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 10 kΩ, See Figure 94		−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 92	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 93		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 10 kΩ, See Figure 92		25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 10 kΩ, See Figure 94		25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 10 kΩ, See Figure 94		−40°C		49°		
				25°C		46°		
				85°C		43°		

HIGH-BIAS MODE

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		− 0.2 to 2	− 0.3 to 2.3		− 0.2 to 4	− 0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	95		70	95		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		− 1.2			− 1.4		μA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		325	1500		675	1600	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	2, 3
α_{VIO}	Input offset voltage temperature coefficient	Distribution	4, 5
V_{OH}	High-level output voltage	vs Output current	6
		vs Supply voltage	7
		vs Temperature	8
V_{OL}	Low-level output voltage	vs Common-mode input voltage	9
		vs Temperature	10, 12
		vs Differential input voltage	11
		vs Low-level output current	13
A_{VD}	Differential voltage amplification	vs Supply voltage	14
		vs Temperature	15
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	16
V_{IC}	Common-mode input voltage	vs Supply voltage	17
I_{DD}	Supply current	vs Supply voltage	18
		vs Temperature	19
SR	Slew rate	vs Supply voltage	20
		vs Temperature	21
	Bias select current	vs Supply voltage	22
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	23
B_1	Gain-bandwidth product	vs Temperature	24
		vs Supply voltage	25
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	26, 27
ϕ_m	Phase margin	vs Supply voltage	28
		vs Temperature	29
		vs Load capacitance	30
V_n	Equivalent input noise voltage	vs Frequency	31

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

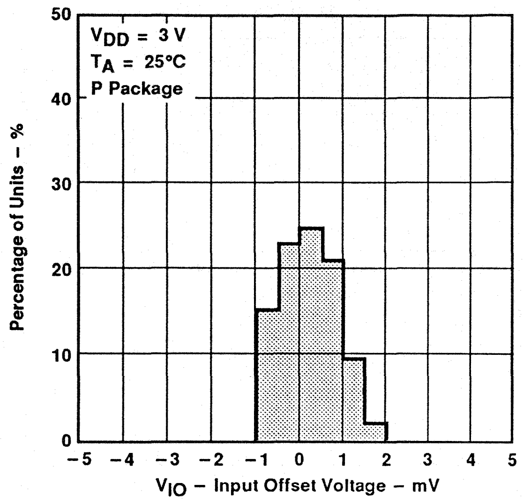


Figure 2

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

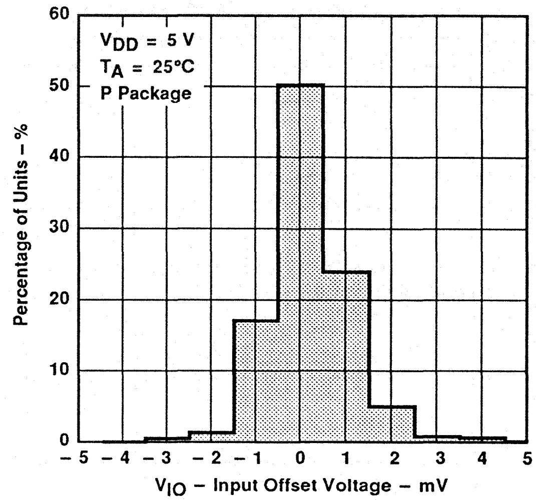


Figure 3

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

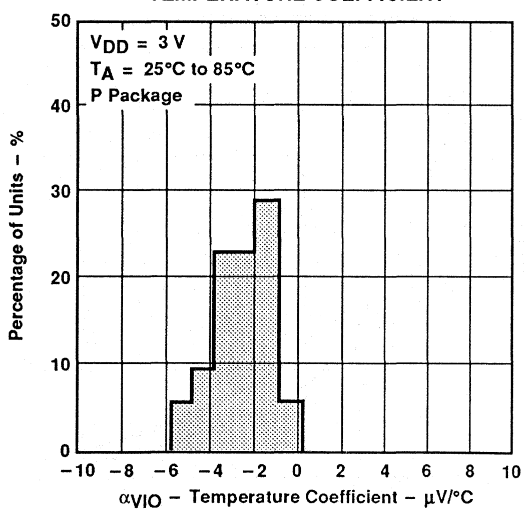


Figure 4

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

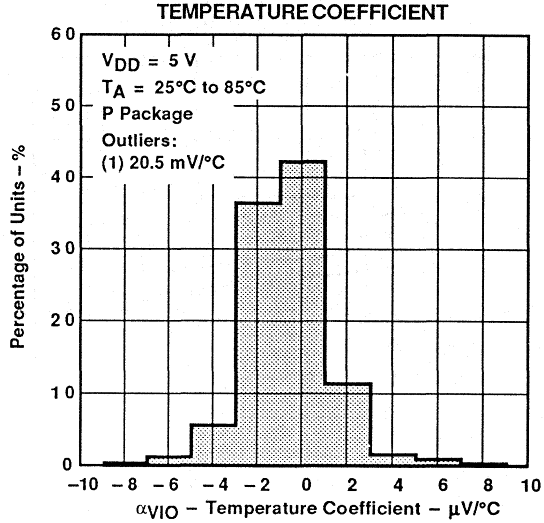


Figure 5

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

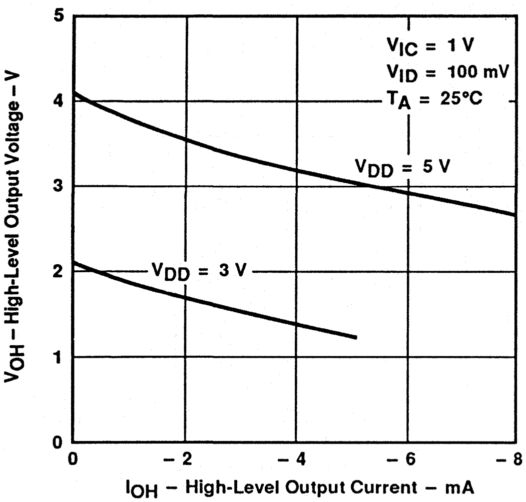


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

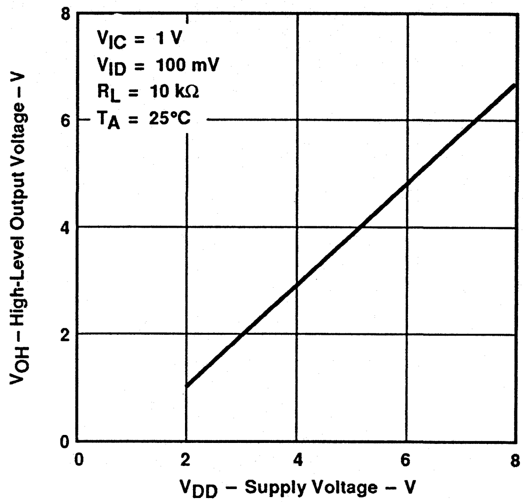


Figure 7

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

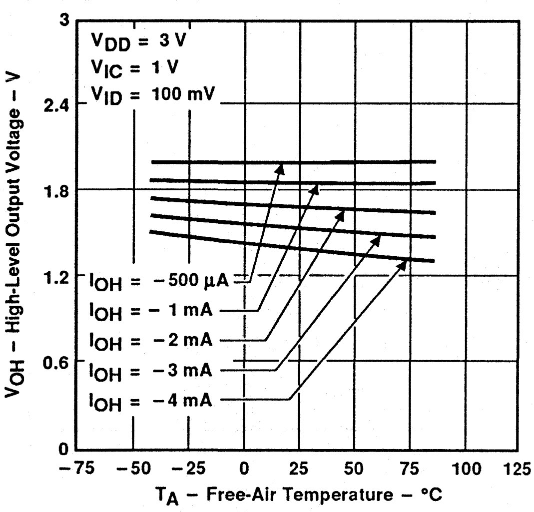


Figure 8
2341.hlov.fat

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

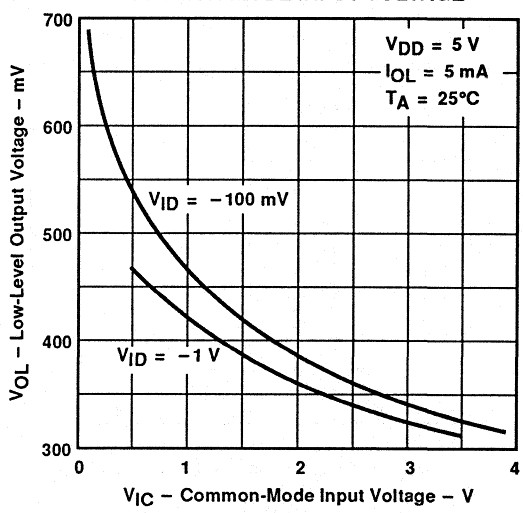


Figure 9

TEXAS INSTRUMENTS

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

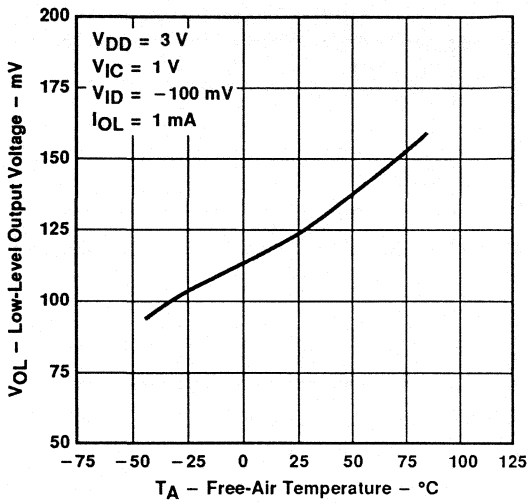


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

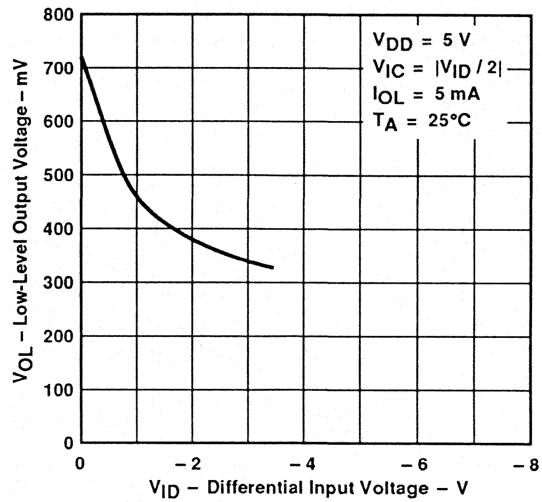


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

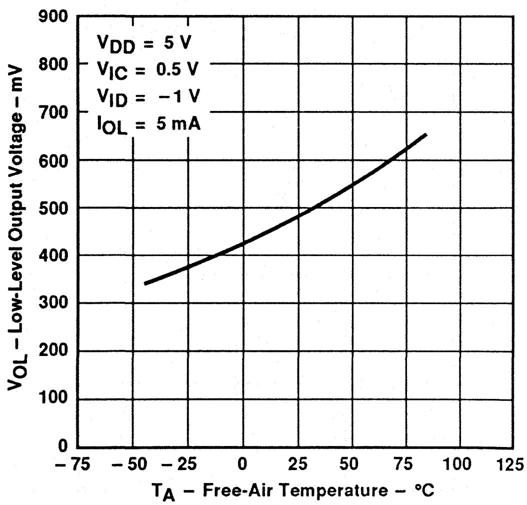


Figure 12

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

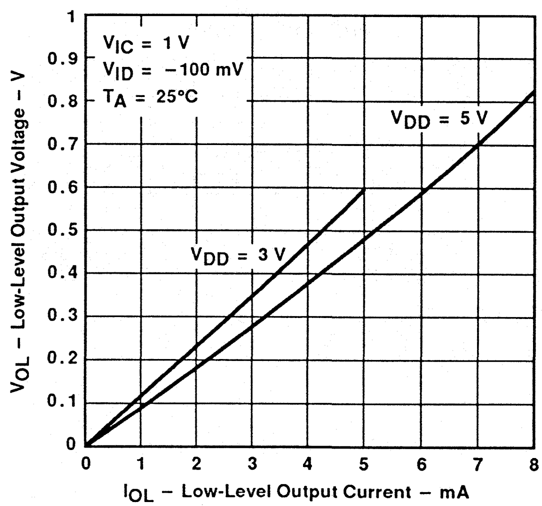


Figure 13

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

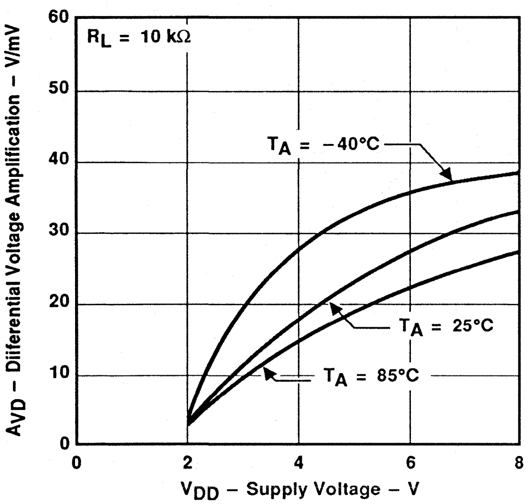


Figure 14

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

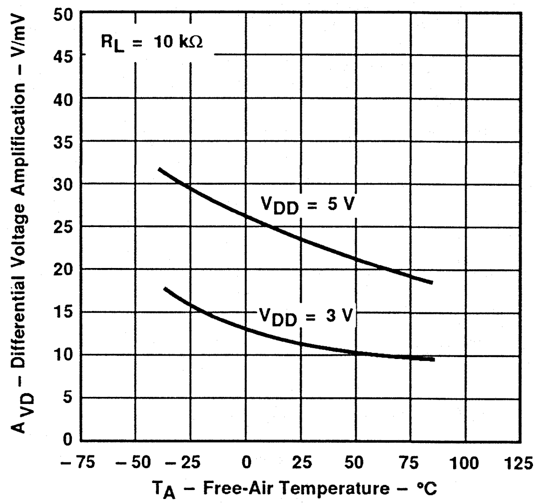


Figure 15

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

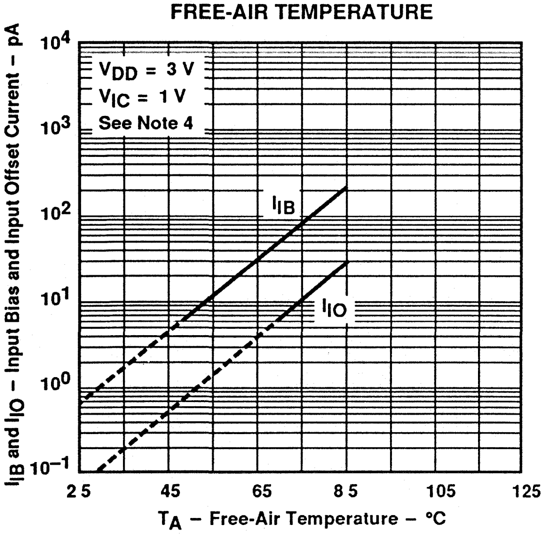


Figure 16

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

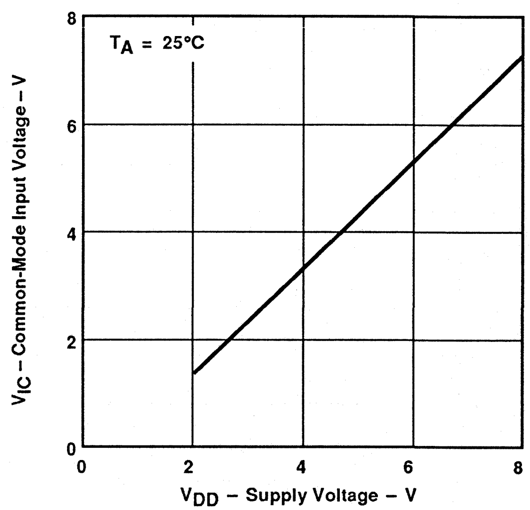


Figure 17

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

SUPPLY CURRENT vs SUPPLY VOLTAGE

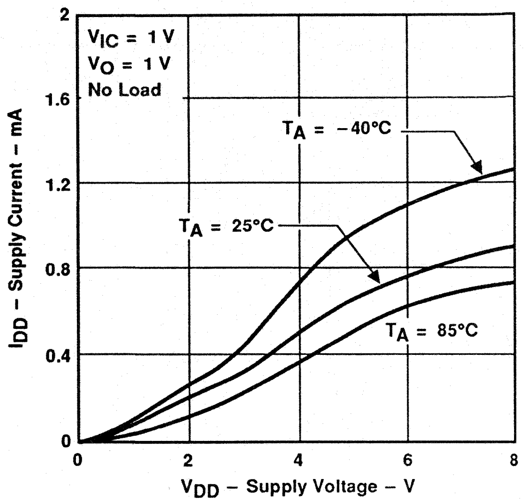


Figure 18

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

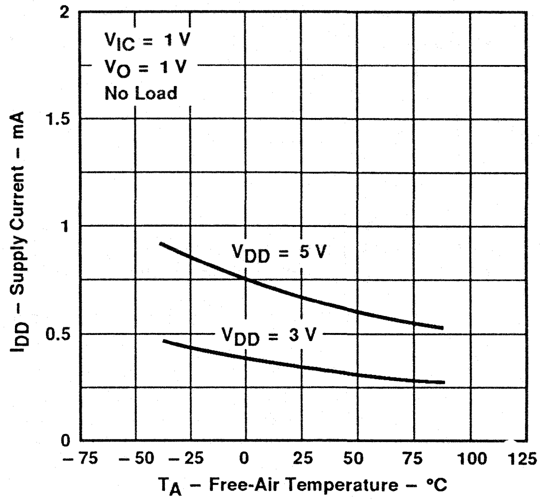


Figure 19

SLEW RATE vs SUPPLY VOLTAGE

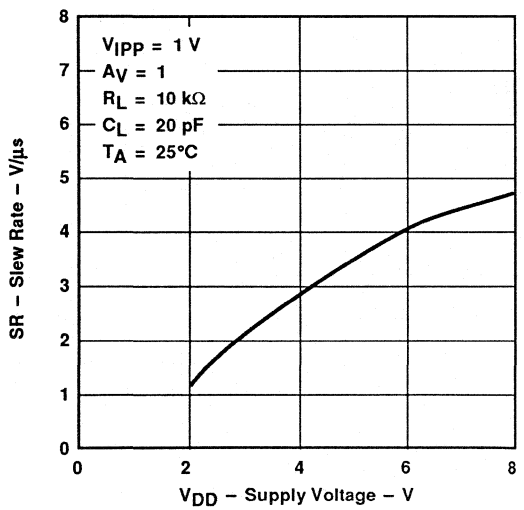


Figure 20

SLEW RATE vs FREE-AIR TEMPERATURE

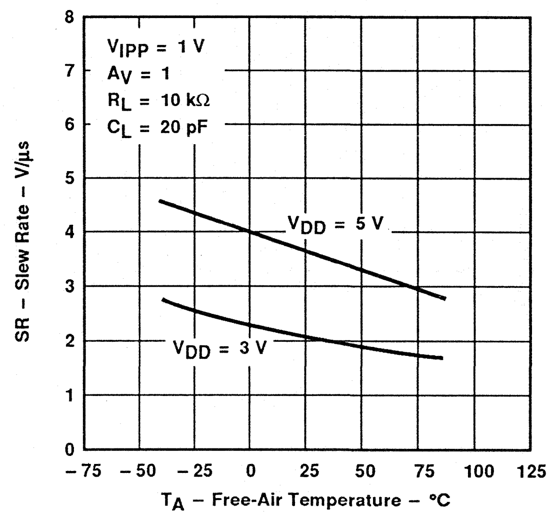


Figure 21

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

BIAS SELECT CURRENT vs SUPPLY VOLTAGE

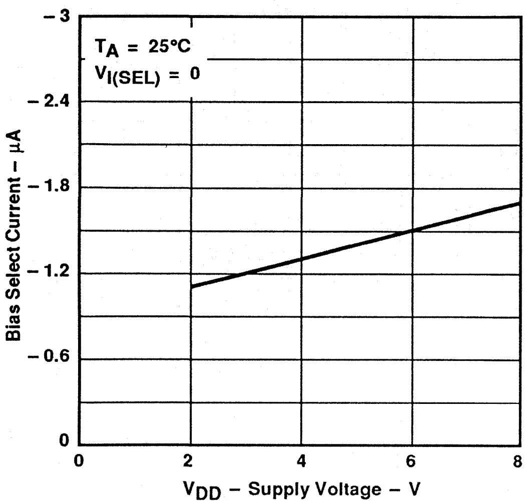


Figure 22

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

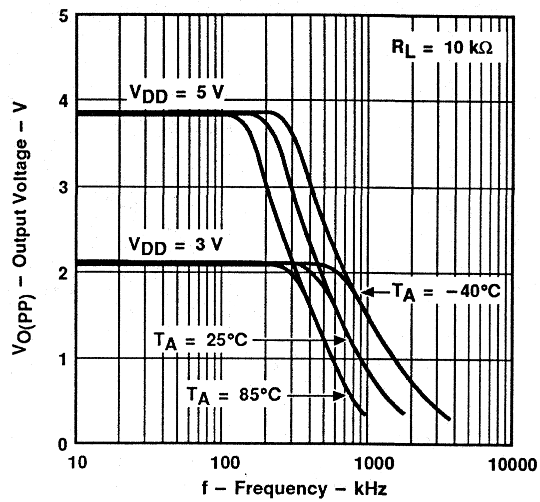


Figure 23

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

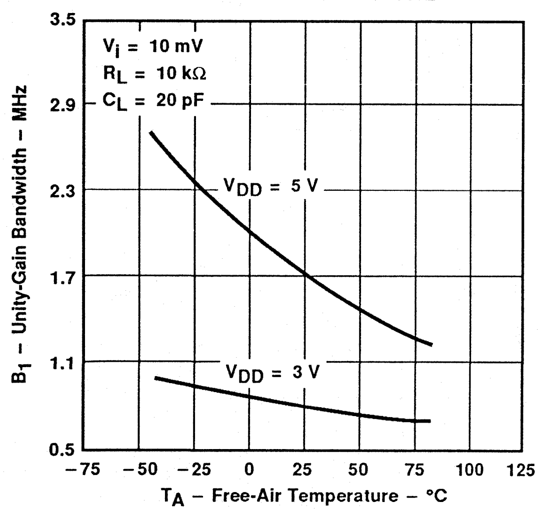


Figure 24

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

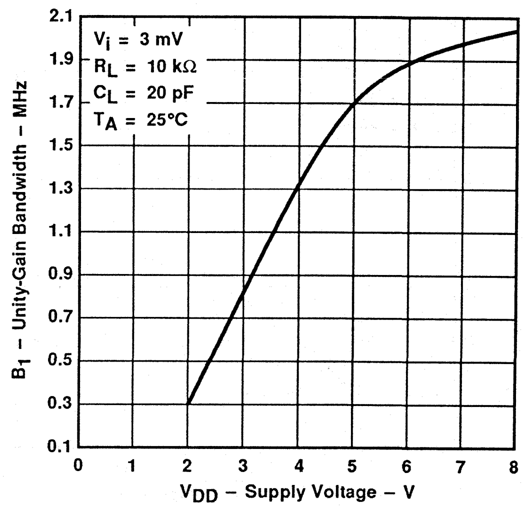


Figure 25

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

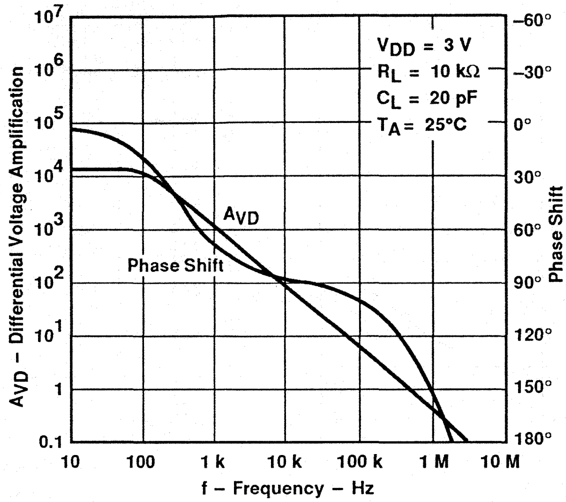


Figure 26

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

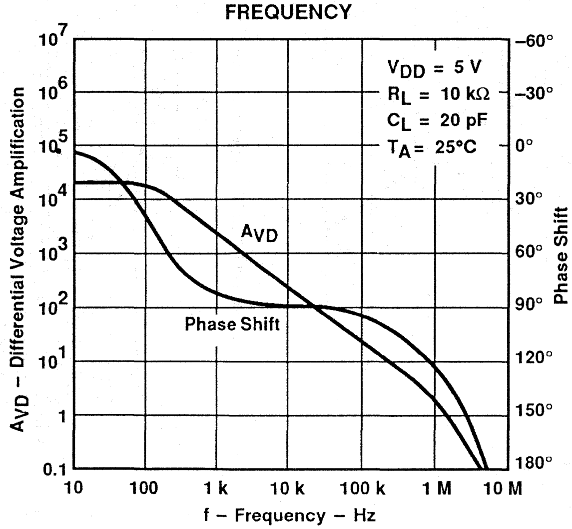


Figure 27

TYPICAL CHARACTERISTICS (HIGH-BIAS MODE)†

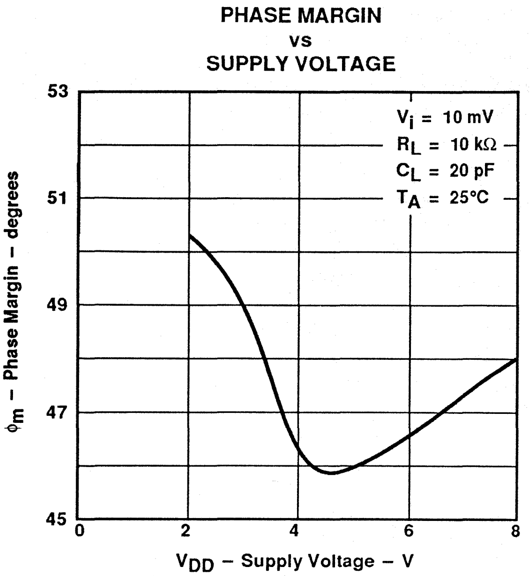


Figure 28

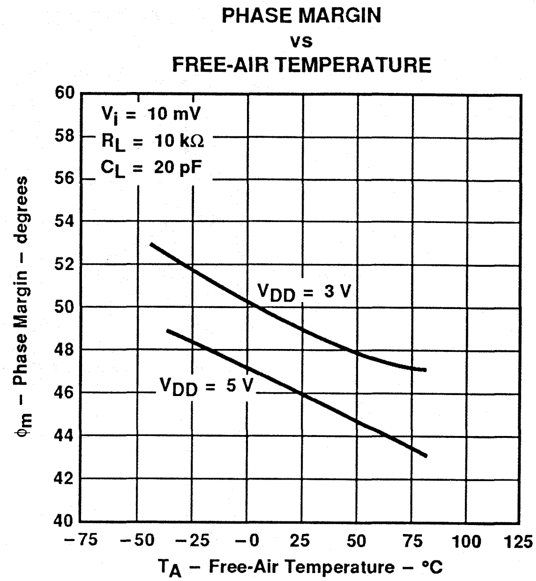


Figure 29

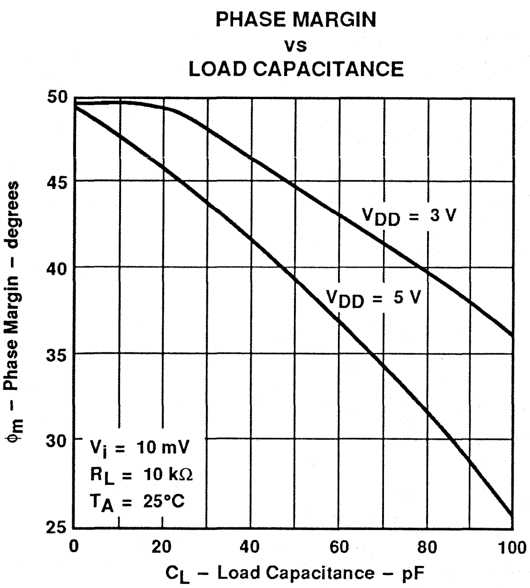


Figure 30

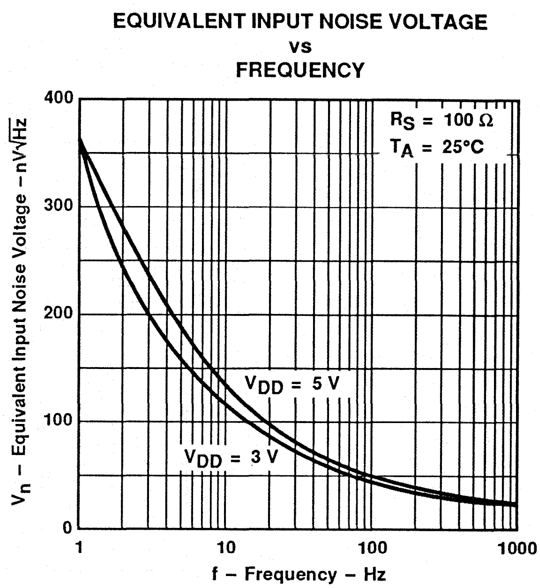


Figure 31

†Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	– 0.2 to 2	– 0.3 to 2.3		– 0.2 to 4	– 0.3 to 4.2		V
			Full range	– 0.2 to 1.8			– 0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = –1 mA	25°C	1.75	1.9		3.2	3.9		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = –100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25°C	25	83		25	170		V/mV
			Full range	15			15			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	92		65	91		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	94		70	94		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		–100			–130		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		65	250		105	280	μA
			Full range			360			400	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

MEDIUM-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 92	V_{IPP} = 1 V	25°C		0.38		V/μs
				85°C		0.29		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 93		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 92		25°C		34		kHz
				85°C		32		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 100 kΩ, See Figure 94		25°C		300		kHz
				85°C		235		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 100 kΩ, See Figure 94		−40°C		42°		
				25°C		39°		
				85°C		36°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 100 kΩ, C_L = 20 pF, See Figure 92	V_{IPP} = 1 V	25°C		0.43		V/μs
				85°C		0.35		
			V_{IPP} = 2.5 V	25°C		0.40		
				85°C		0.32		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 93		25°C		32		nV/√Hz
B_{OM}	Maximum output swing bandwidth	$V_O = V_{OH}$, C_L = 20 pF, R_L = 100 kΩ, See Figure 92		25°C		55		kHz
				85°C		45		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 100 kΩ, See Figure 94		25°C		525		kHz
				85°C		370		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 100 kΩ, See Figure 94		−40°C		43°		
				25°C		40°		
				85°C		38°		

MEDIUM-BIAS MODE

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 100 kΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.9		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 100 kΩ, See Note 6	25	83		25	170		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	92		65	91		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	94		70	94		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		−100			−130		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		65	250		105	280	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

table of graphs

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		vs Temperature	38
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		vs Low-level output current	43
A_{VD}	Differential voltage amplification	vs Supply voltage	44
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I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	46
V_{IC}	Common-mode input voltage	vs Supply voltage	47
I_{DD}	Supply current	vs Supply voltage	48
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SR	Slew rate	vs Supply voltage	50
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B_1	Gain-bandwidth product	vs Temperature	54
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A_{VD}	Differential voltage amplification and phase shift	vs Frequency	56, 57
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		vs Load capacitance	60
V_n	Equivalent input noise voltage	vs Frequency	61

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

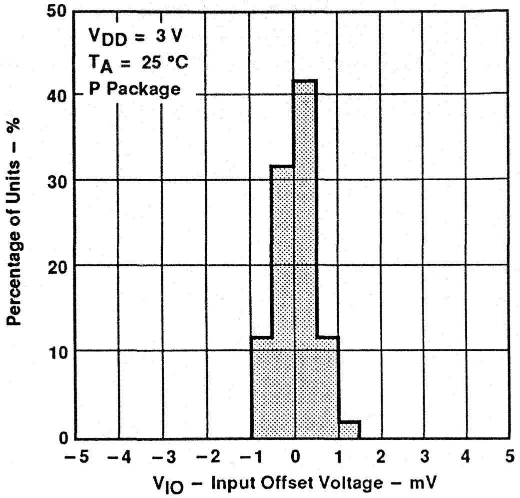


Figure 32

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

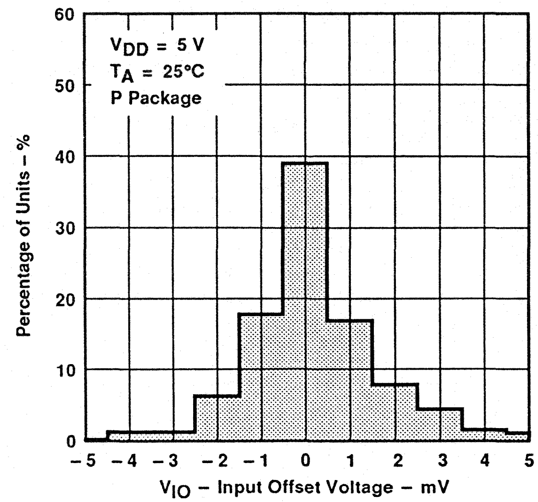


Figure 33

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

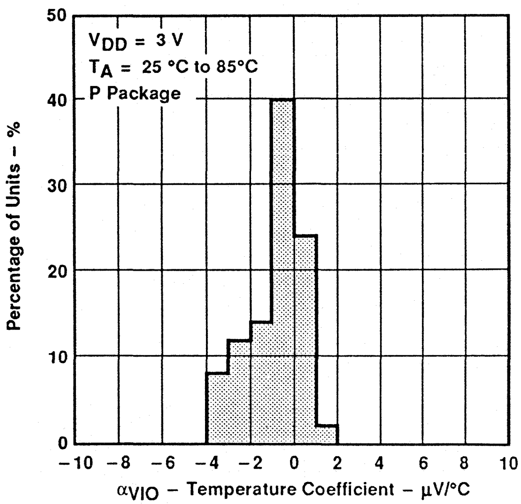


Figure 34

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

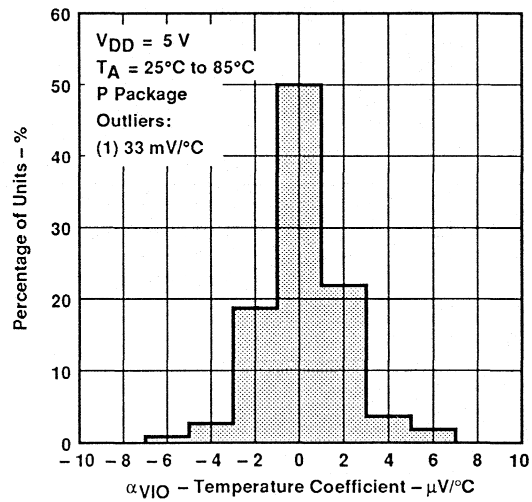


Figure 35

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

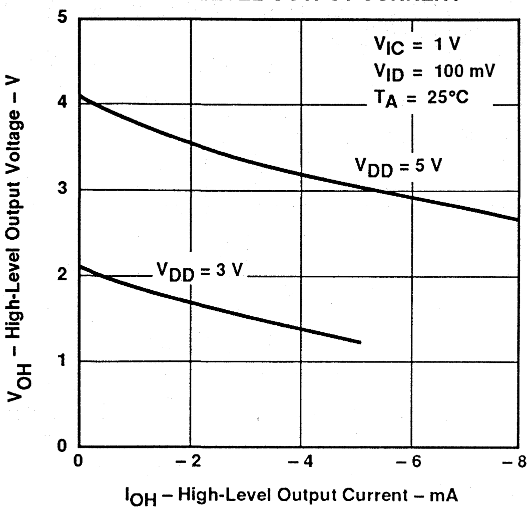


Figure 36

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

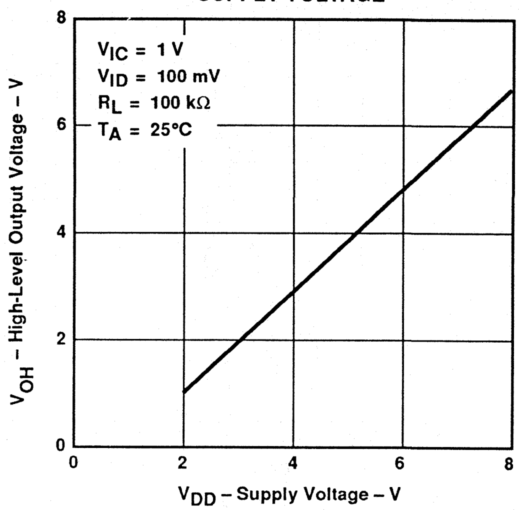


Figure 37

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

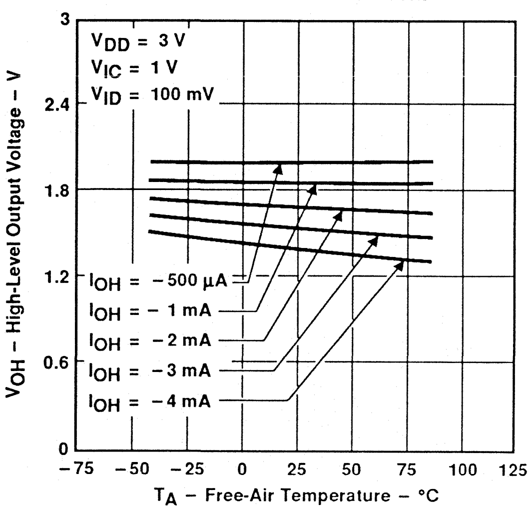


Figure 38

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

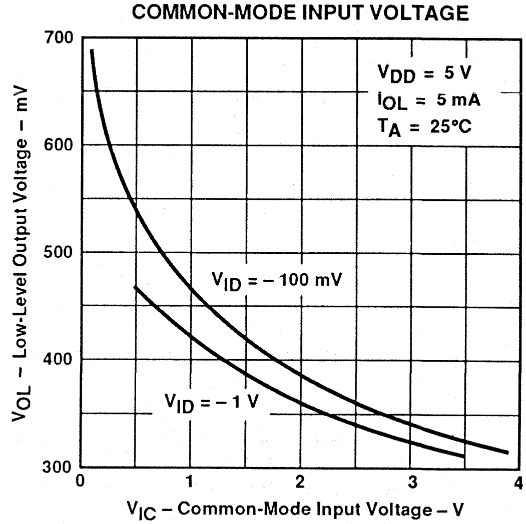


Figure 39

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

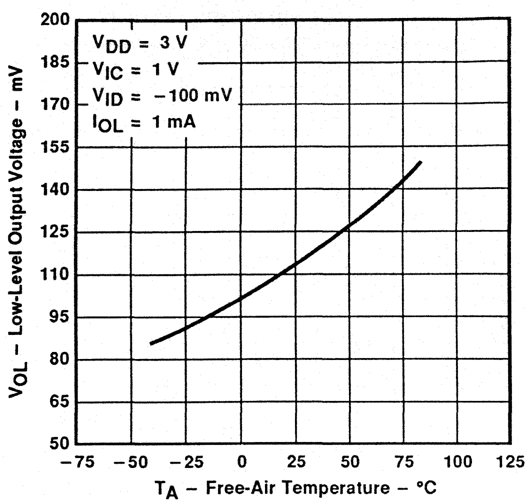


Figure 40

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

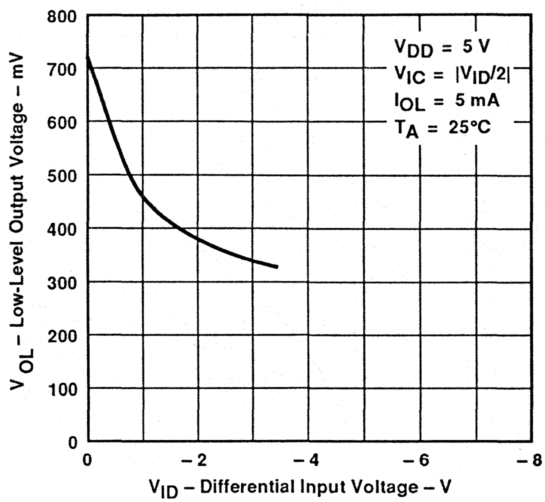


Figure 41

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

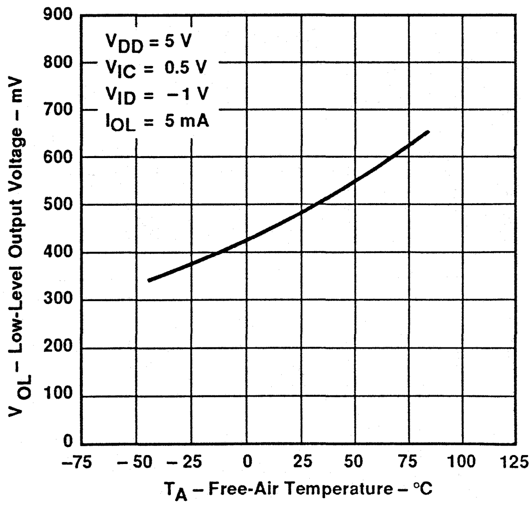


Figure 42

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

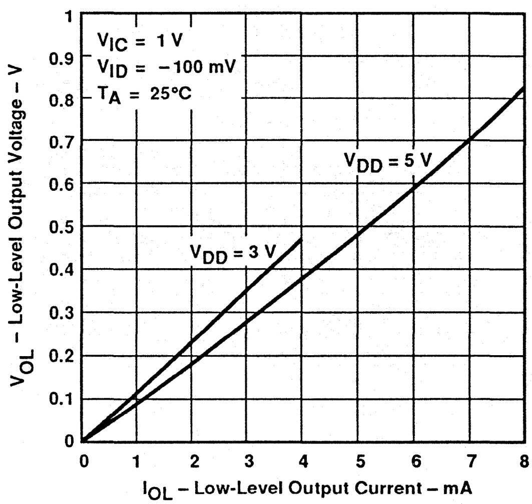


Figure 43

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

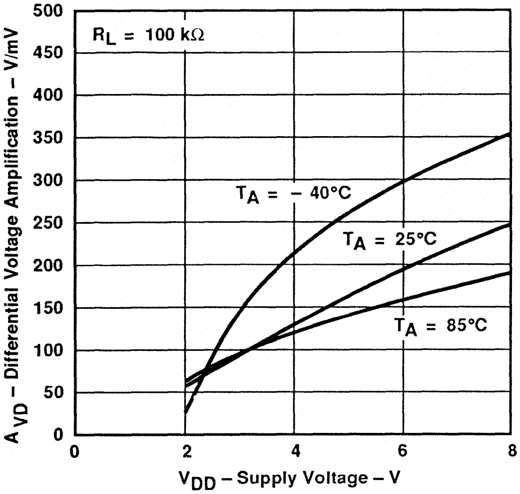


Figure 44

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

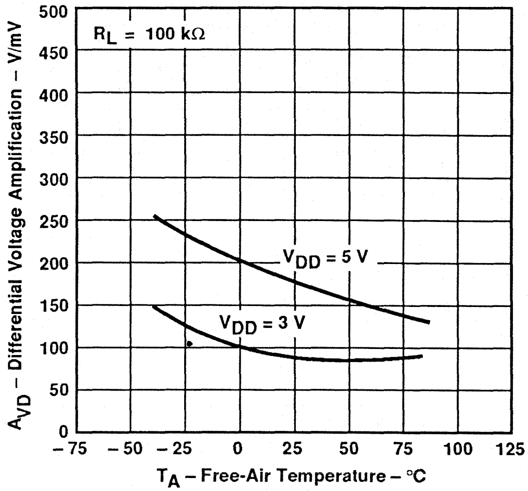


Figure 45

INPUT BIAS CURRENT AND INPUT
OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

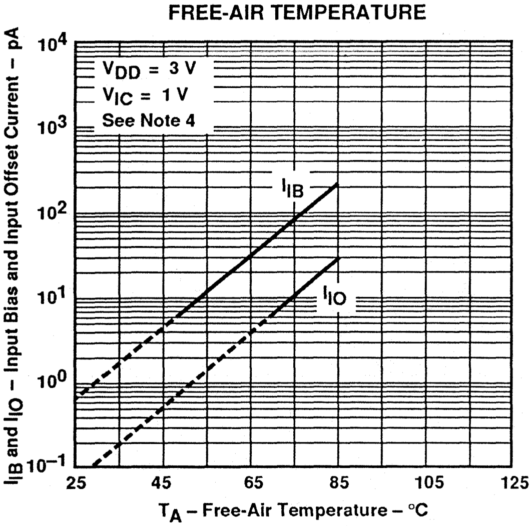


Figure 46

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

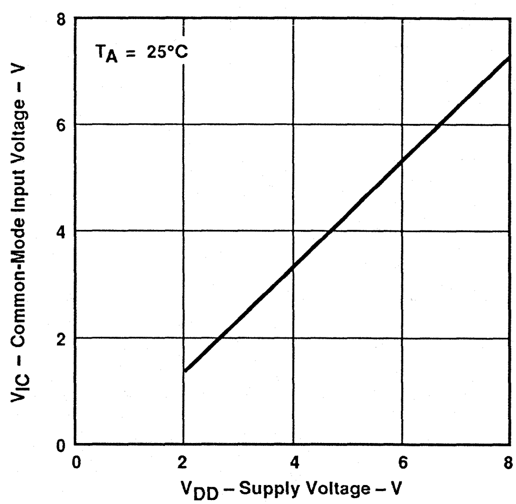


Figure 47

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

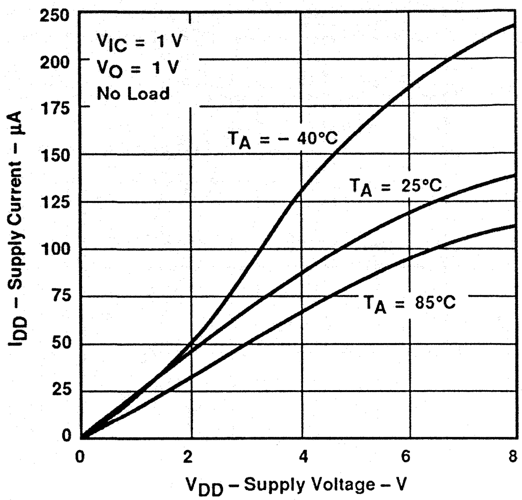


Figure 48

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

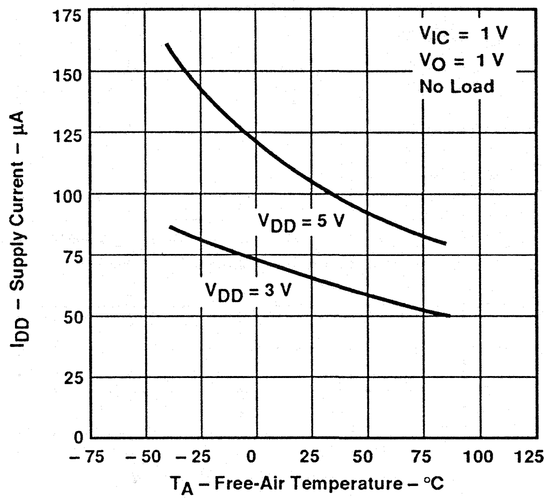


Figure 49

SLEW RATE
vs
SUPPLY VOLTAGE

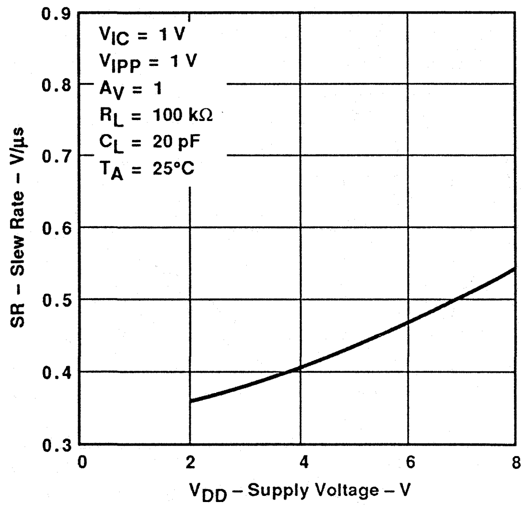


Figure 50

SLEW RATE
vs
FREE-AIR TEMPERATURE

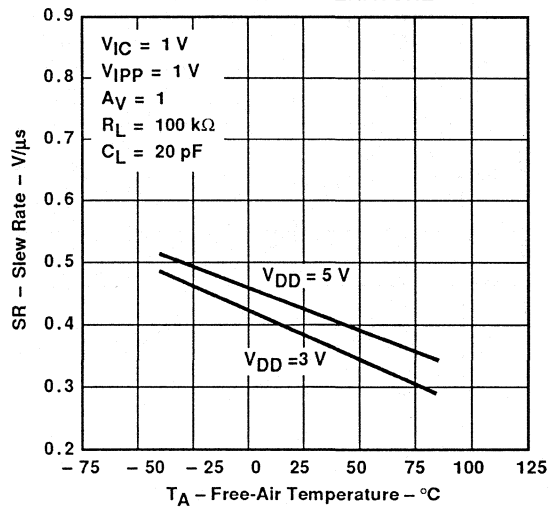


Figure 51

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

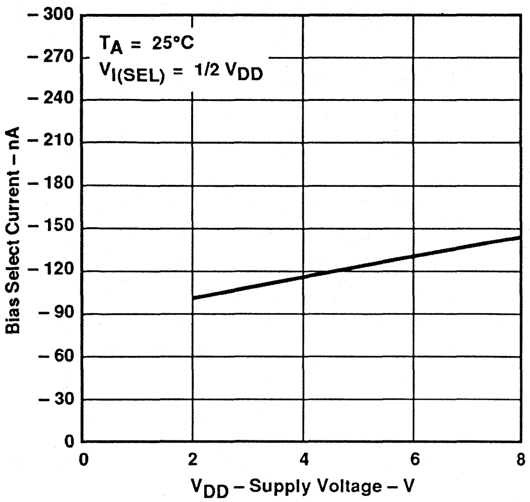


Figure 52

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

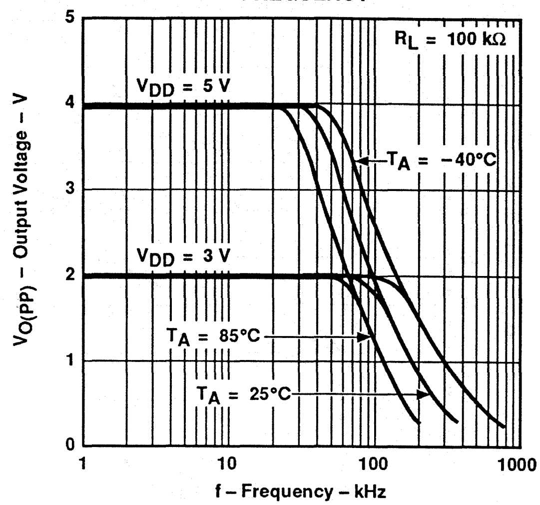


Figure 53

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

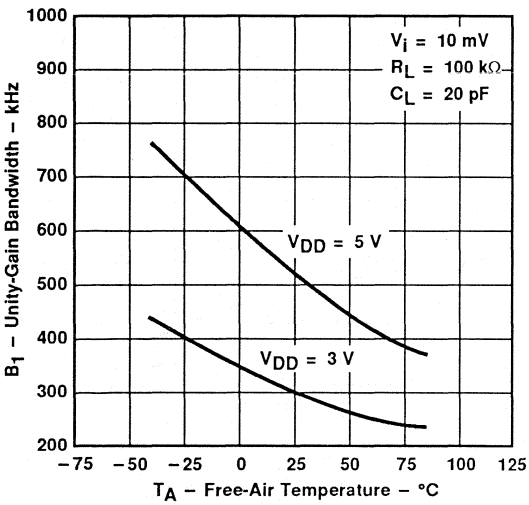


Figure 54

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

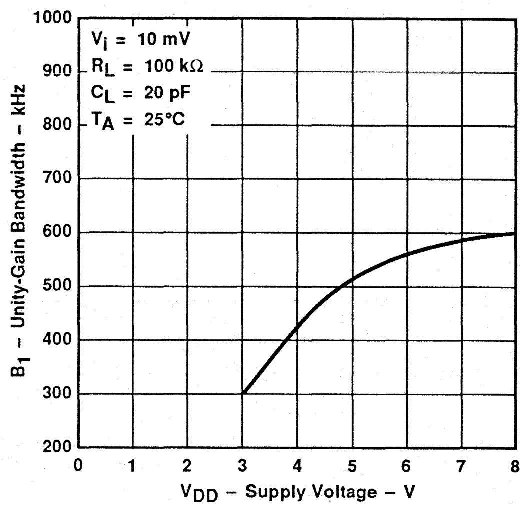


Figure 55

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

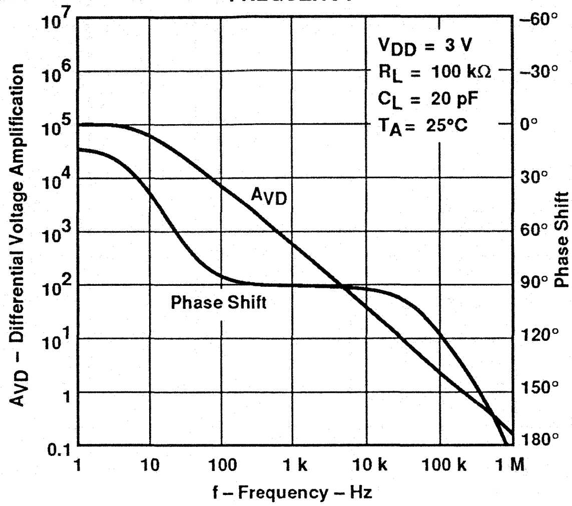


Figure 56

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

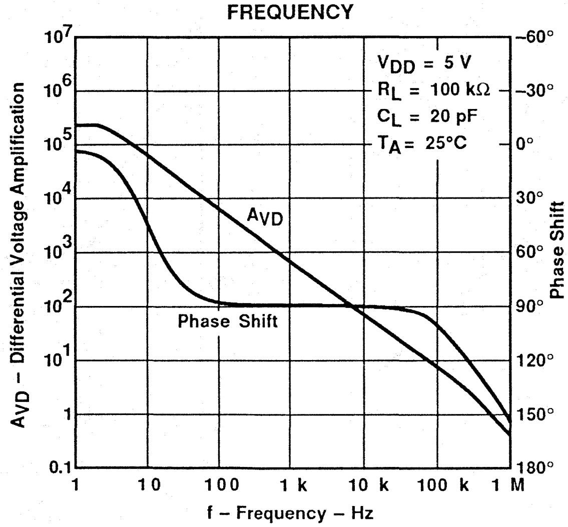


Figure 57

TYPICAL CHARACTERISTICS (MEDIUM-BIAS MODE)

PHASE MARGIN vs SUPPLY VOLTAGE

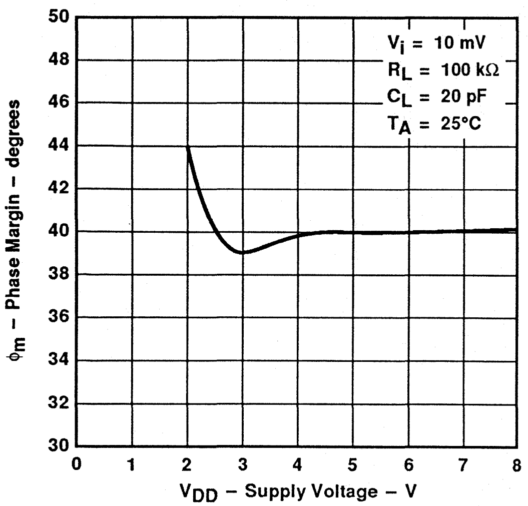


Figure 58

PHASE MARGIN vs FREE-AIR TEMPERATURE

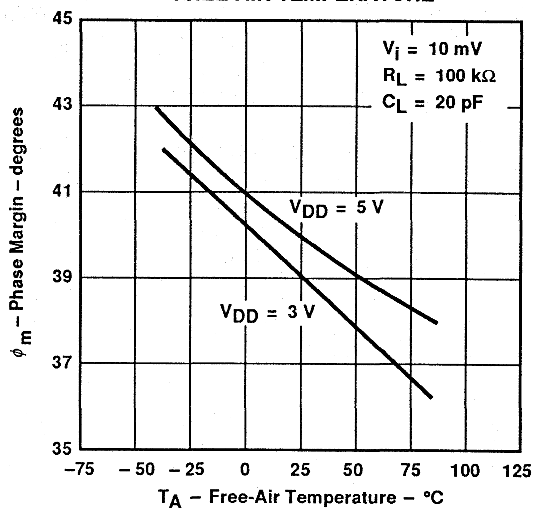


Figure 59

PHASE MARGIN vs LOAD CAPACITANCE

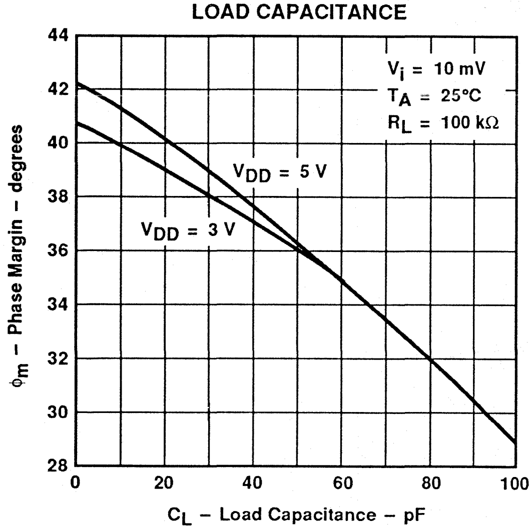


Figure 60

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

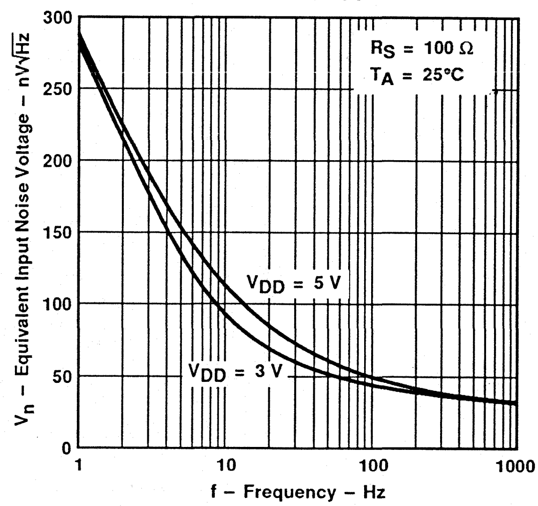


Figure 61

LOW-BIAS MODE

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V MIN	V_{DD} = 3 V TYP	V_{DD} = 3 V MAX	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ	25°C		0.6	8		1.1	8	mV
			Full range			10			10	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		1			1.1		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.8		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		115	150		95	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	25°C	50	400		50	520		V/mV
			Full range	50			50			
CMRR	Common-mode rejection ratio	V_O = 1 V, $V_{IC} = V_{ICR}$min, R_S = 50 Ω	25°C	65	88		65	94		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	86		70	86		dB
			Full range	65			65			
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0	25°C		10			65		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load	25°C		5	17		10	17	μA
			Full range			27			27	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

6. At V_{DD} = 5 V, V_{OPP} = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

LOW-BIAS MODE

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 92	V_{IPP} = 1 V	25°C		0.02		V/μs
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 93		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 92		25°C		2.5		kHz
				85°C		2		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 1 MΩ, See Figure 94		25°C		27		kHz
				85°C		21		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 1 MΩ, See Figure 94		−40°C		39°		
				25°C		34°		
				85°C		28°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 1 MΩ, C_L = 20 pF, See Figure 92	V_{IPP} = 1 V	25°C		0.03		V/μs
				85°C		0.03		
			V_{IPP} = 2.5 V	25°C		0.03		
				85°C		0.02		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 93		25°C		68		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 1 MΩ, See Figure 92		25°C		5		kHz
				85°C		4		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 1 MΩ, See Figure 94		25°C		85		kHz
				85°C		55		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 1 MΩ, See Figure 94		−40°C		38°		
				25°C		34°		
				85°C		28°		

LOW-BIAS MODE

electrical characteristics at sified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 1 MΩ		0.6	8		1.1	8	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		− 0.2 to 2	− 0.3 to 2.3		− 0.2 to 4	− 0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.8		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = − 100 mV, I_{OL} = 1 mA		115	150		95	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 1 MΩ, See Note 6	50	400		50	520		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	88		65	94		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	86		70	86		dB
$I_{I(SEL)}$	Bias select current	$V_{I(SEL)}$ = 0		10			65		nA
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		5	17		10	17	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

table of graphs

			FIGURE
V_{IO}	Input offset voltage	Distribution	62, 63
α_{VIO}	Input offset voltage temperature coefficient	Distribution	64, 65
V_{OH}	High-level output voltage	vs Output current	66
		vs Supply voltage	67
		vs Temperature	68
V_{OL}	Low-level output voltage	vs Common-mode input voltage	69
		vs Temperature	70, 72
		vs Differential input voltage	71
		vs Low-level output current	73
A_{VD}	Differential voltage amplification	vs Supply voltage	74
		vs Temperature	75
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	76
V_{IC}	Common-mode input voltage	vs Supply voltage	77
I_{DD}	Supply current	vs Supply voltage	78
		vs Temperature	79
SR	Slew rate	vs Supply voltage	80
		vs Temperature	81
	Bias select current	vs Supply voltage	82
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	83
B_1	Gain-bandwidth product	vs Temperature	84
		vs Supply voltage	85
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	86, 87
ϕ_m	Phase margin	vs Supply voltage	88
		vs Temperature	89
		vs Load capacitance	80
V_n	Equivalent input noise voltage	vs Frequency	91

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

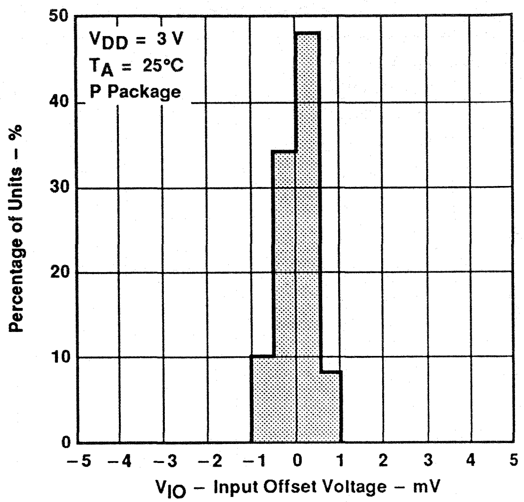


Figure 62

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE

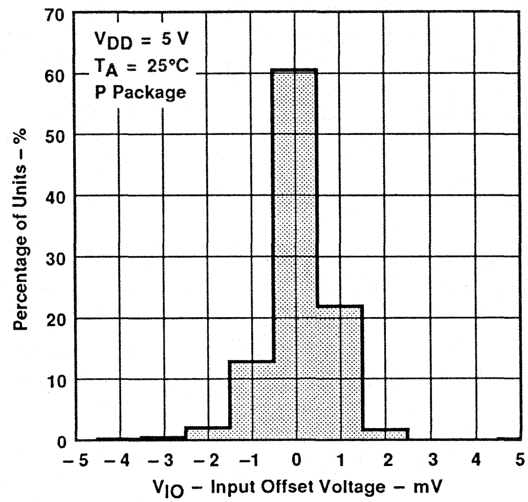


Figure 63

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

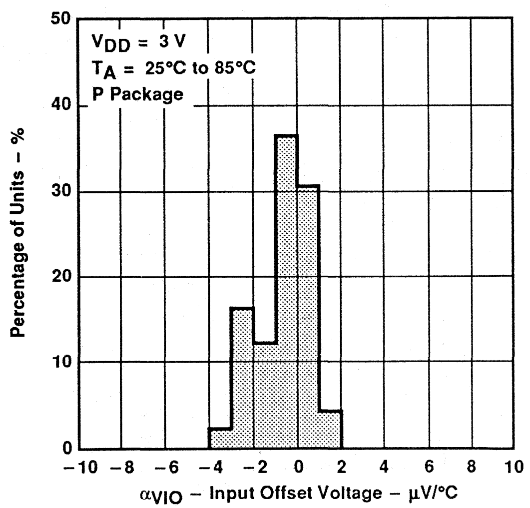


Figure 64

DISTRIBUTION OF TLV2341
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

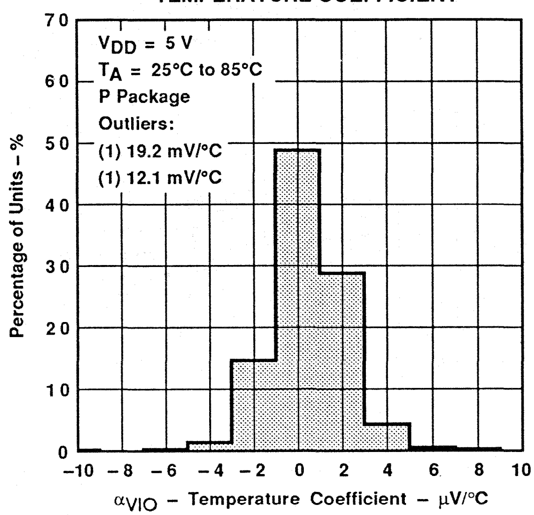


Figure 65

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

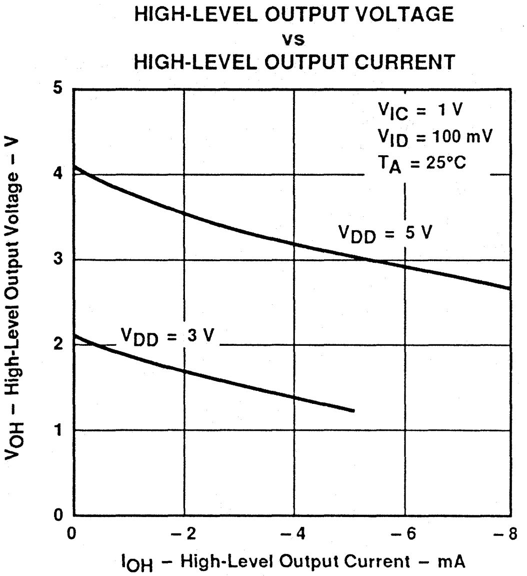


Figure 66

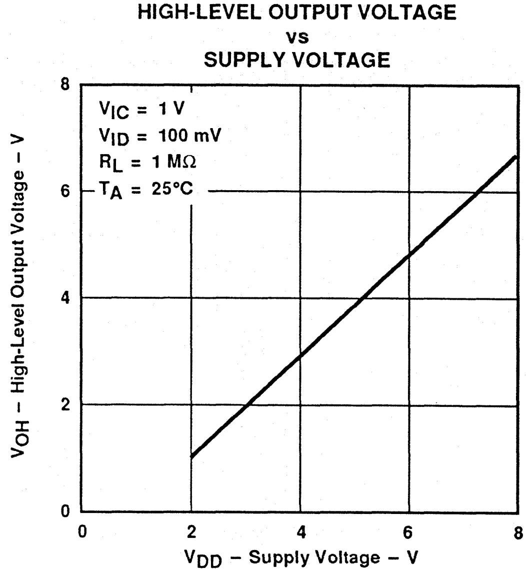


Figure 67

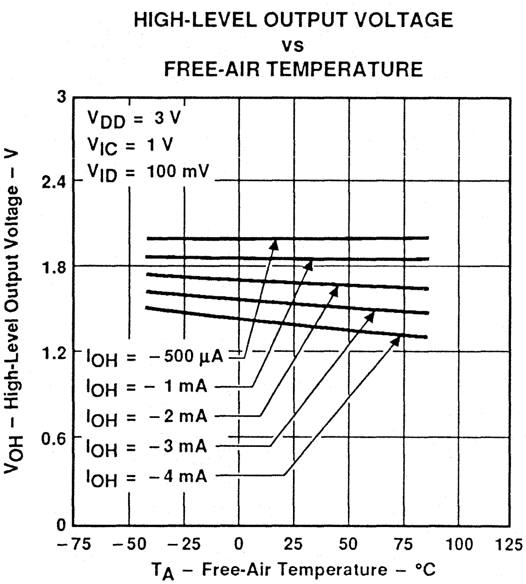


Figure 68

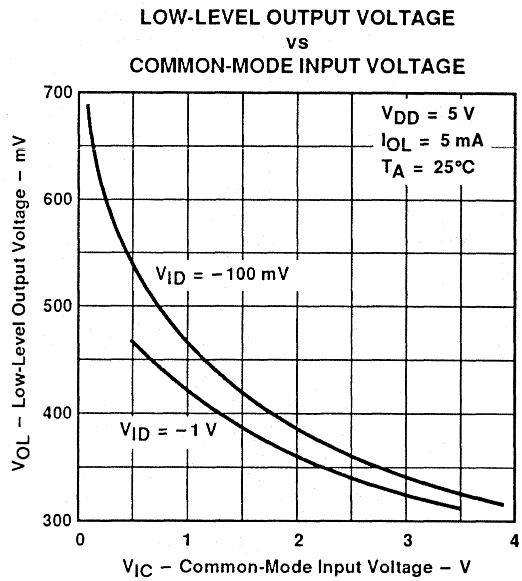


Figure 69

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

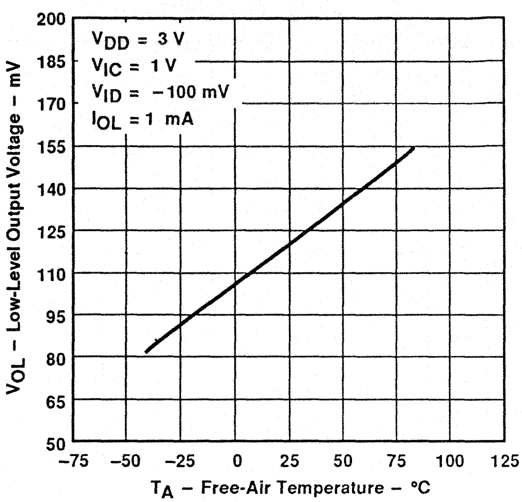


Figure 70

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

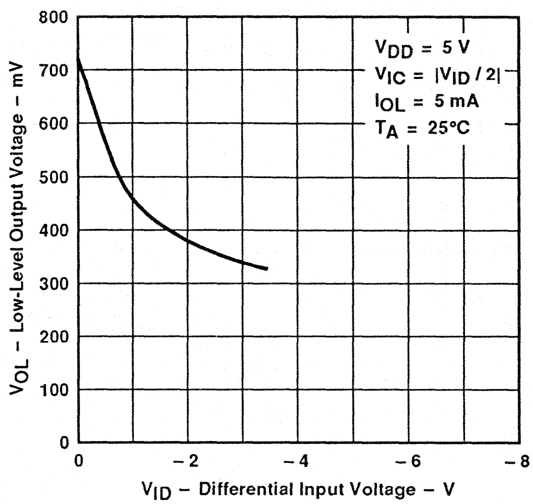


Figure 71

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

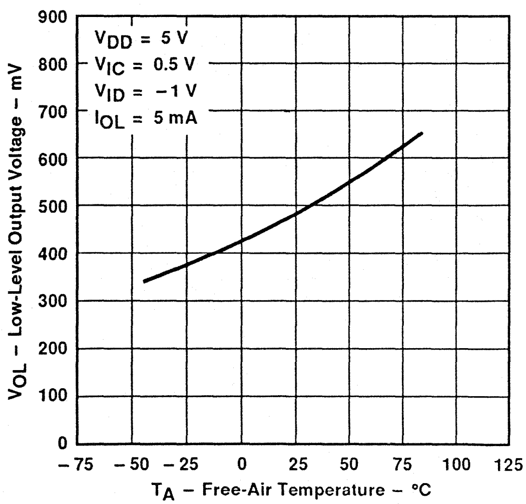


Figure 72

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

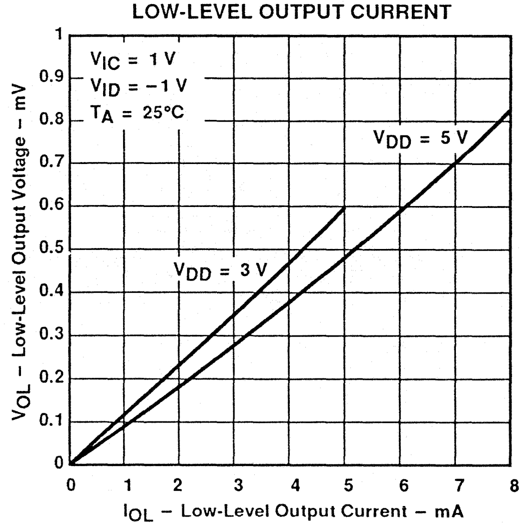


Figure 73

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

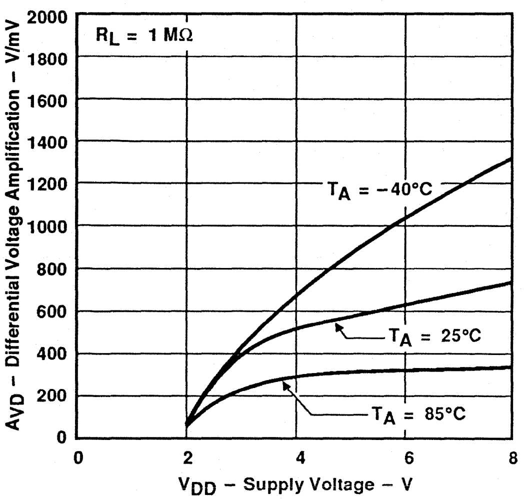


Figure 74

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

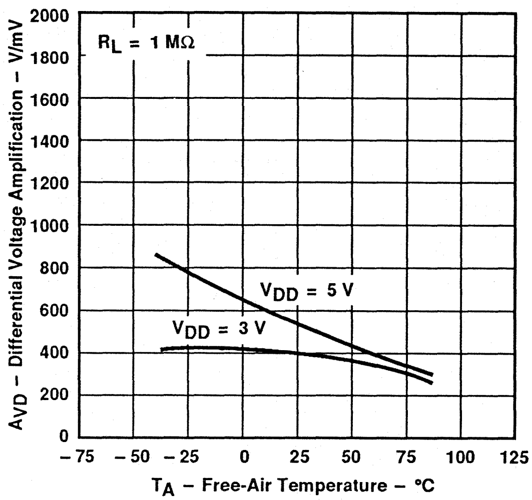


Figure 75

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT
vs
FREE-AIR TEMPERATURE

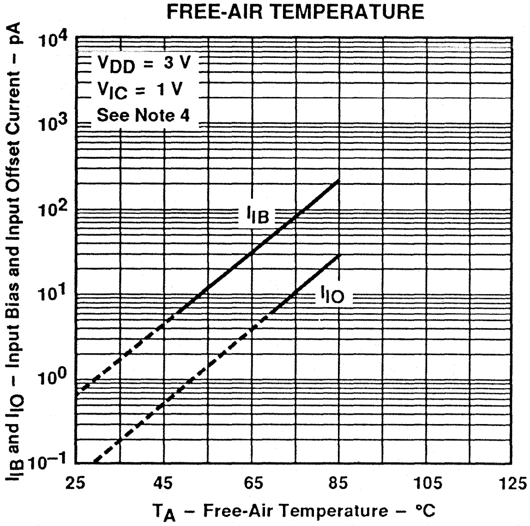


Figure 76

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

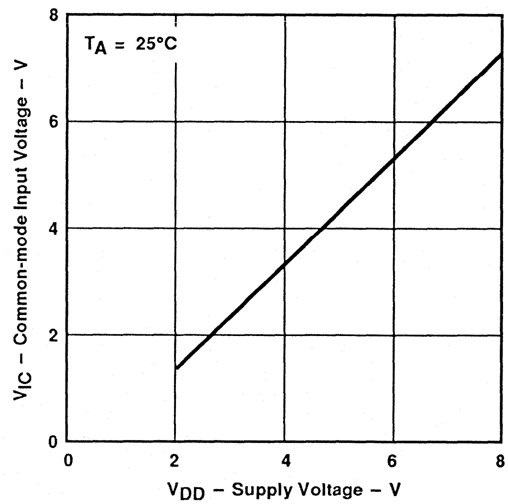


Figure 77

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

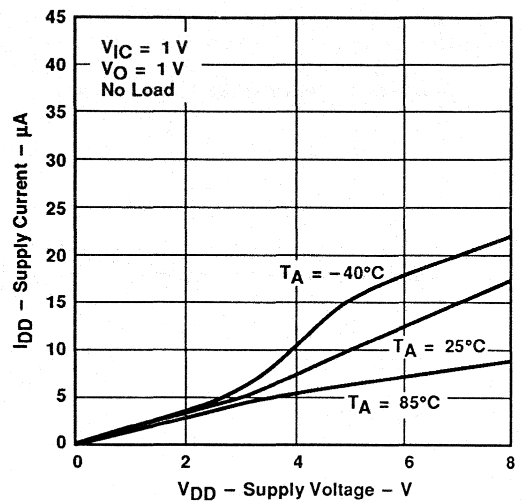


Figure 78

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

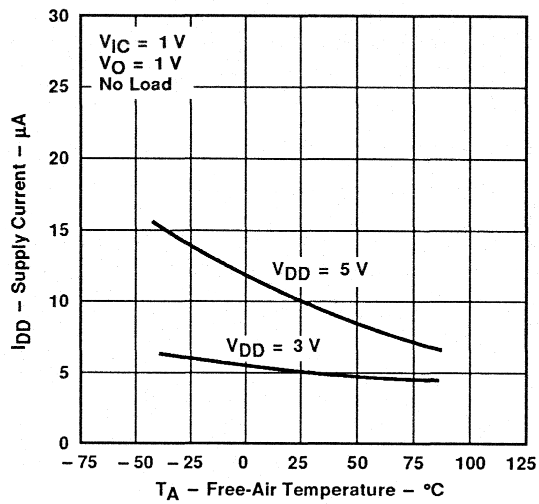


Figure 79

SLEW RATE
vs
SUPPLY VOLTAGE

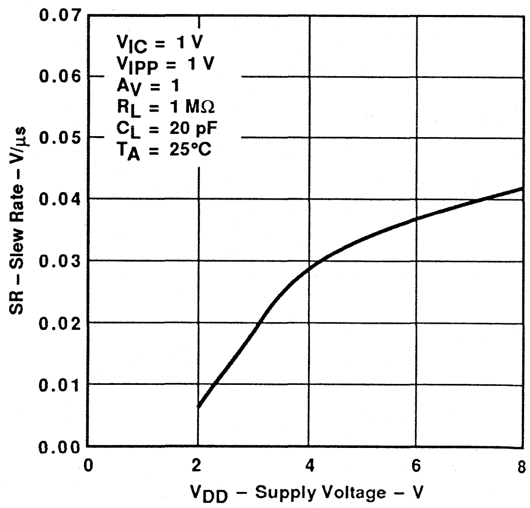


Figure 80

SLEW RATE
vs
FREE-AIR TEMPERATURE

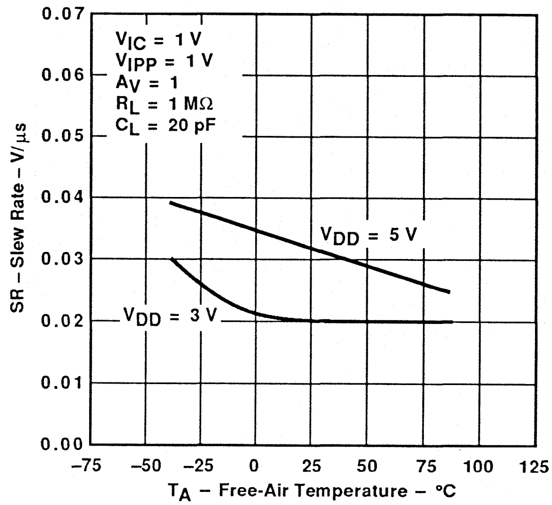


Figure 81

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

BIAS SELECT CURRENT
vs
SUPPLY VOLTAGE

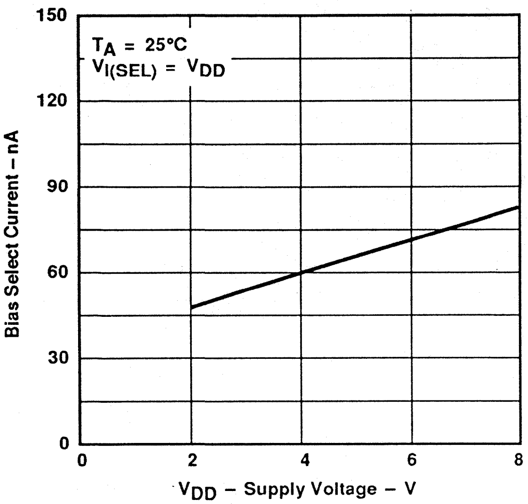


Figure 82

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

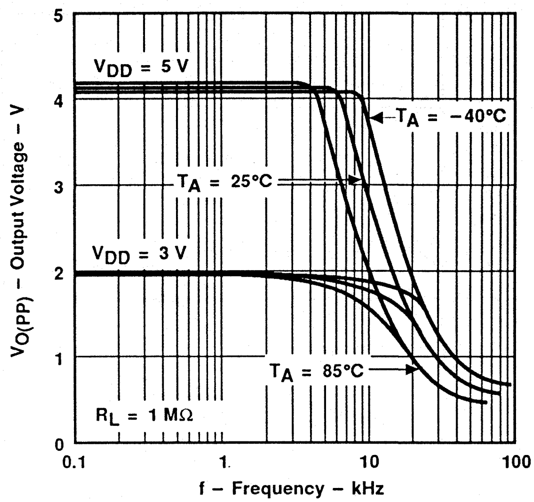


Figure 83

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

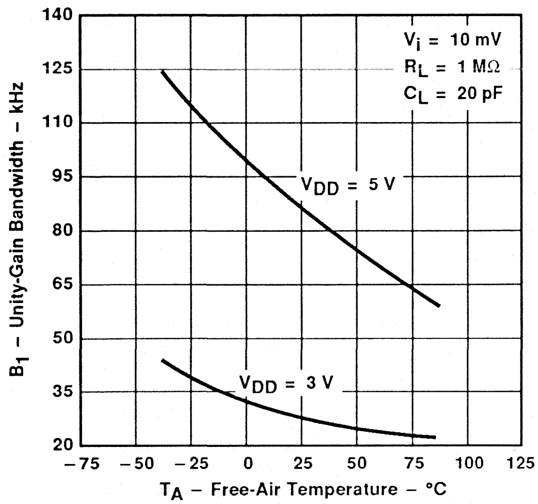


Figure 84

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

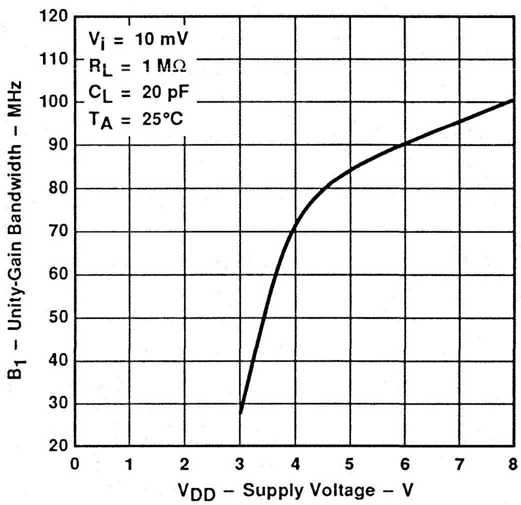


Figure 85

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

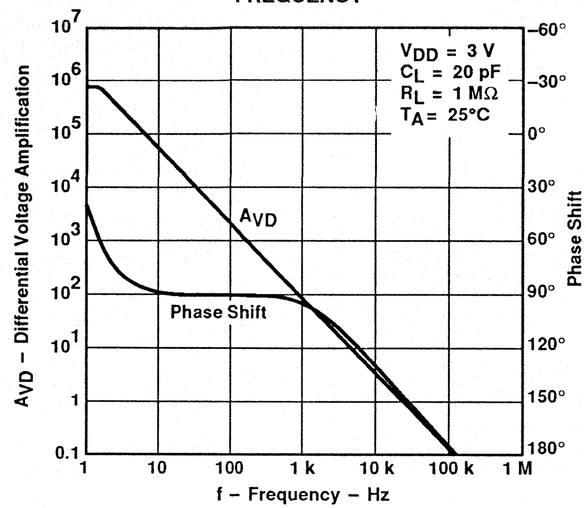


Figure 86

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

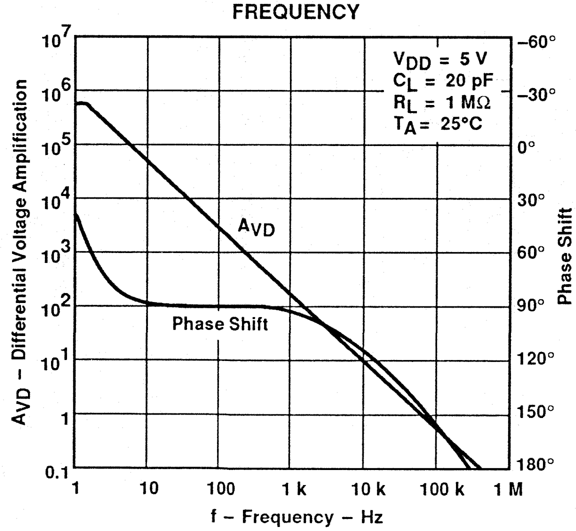


Figure 87

TYPICAL CHARACTERISTICS (LOW-BIAS MODE)

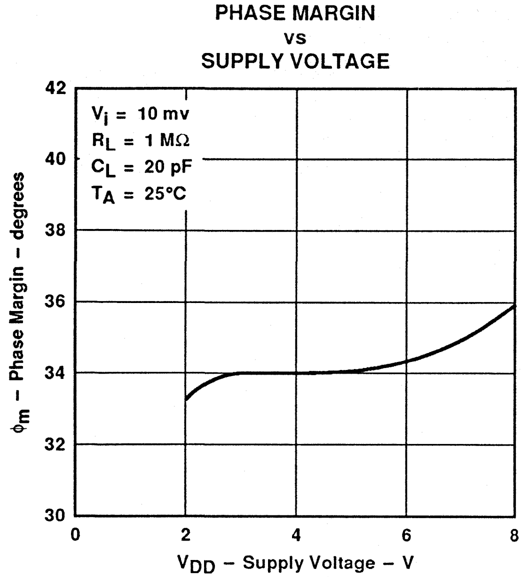


Figure 88

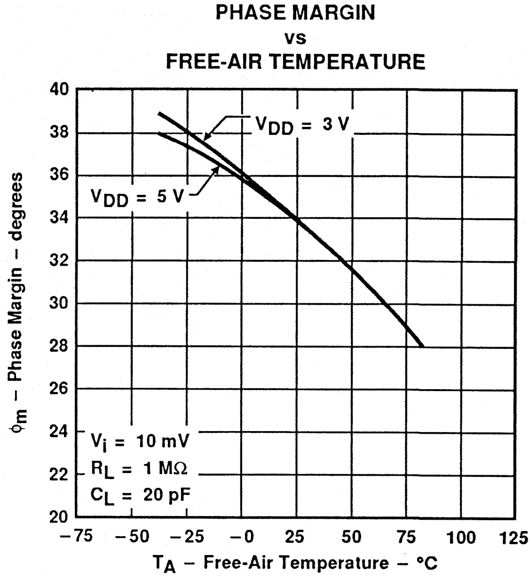


Figure 89

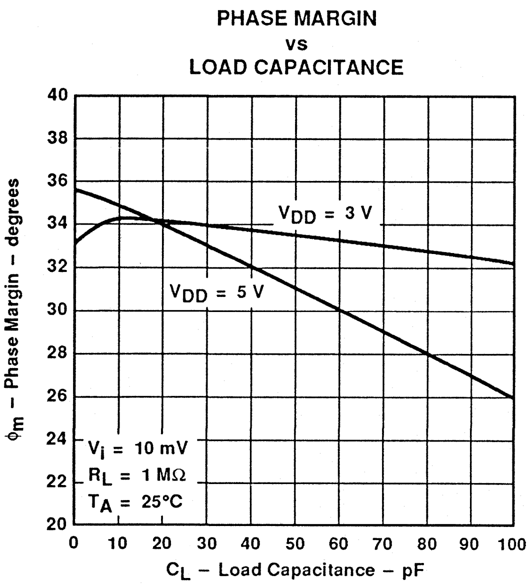


Figure 90

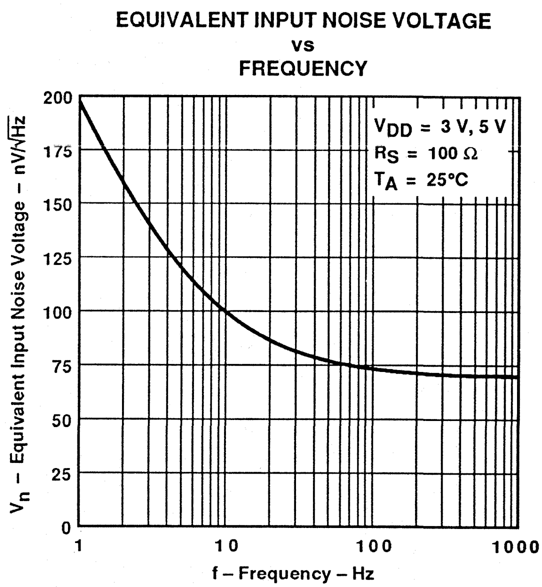
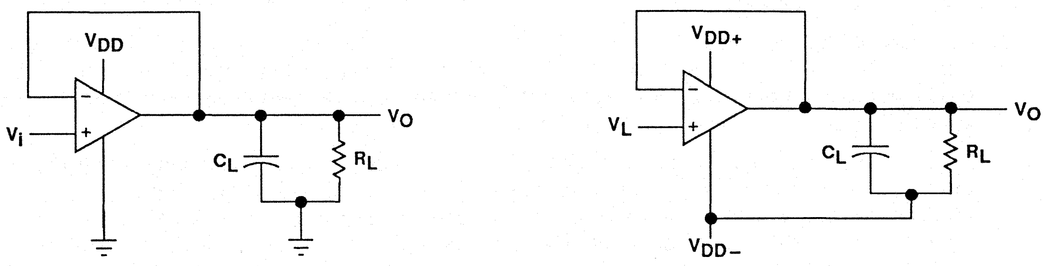


Figure 91

PARAMETER MEASUREMENT INFORMATION

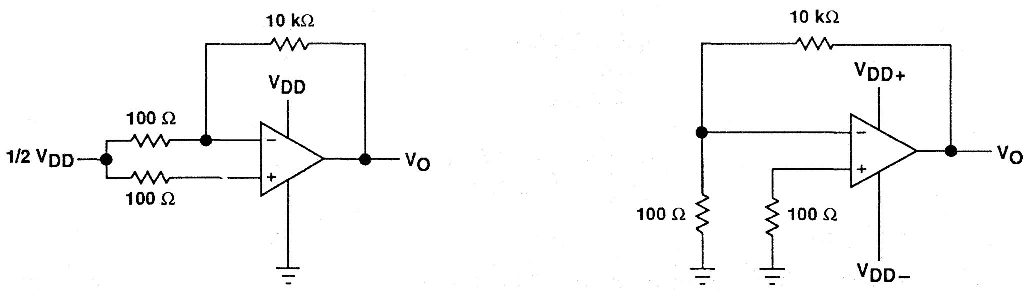
single-supply versus split-supply test circuits

Because the TLV2341 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



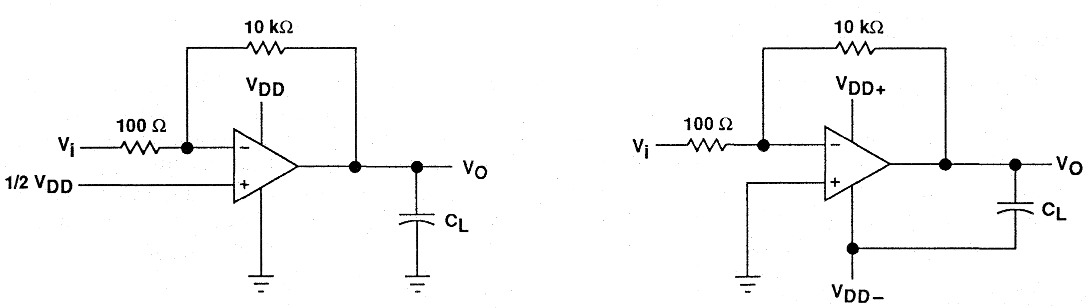
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 92. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 93. Noise Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 94. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2341 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 95). Leakages that would otherwise flow to the inputs will be shunted away.
2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

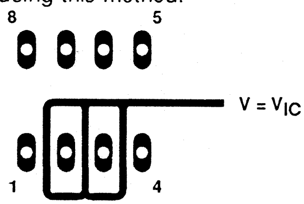


Figure 95. Isolation Metal Around Device Inputs
(P Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 92. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 96). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.

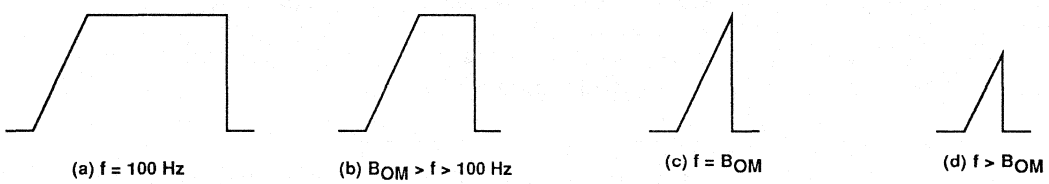


Figure 96. Full-Power-Response Output Signal

test time

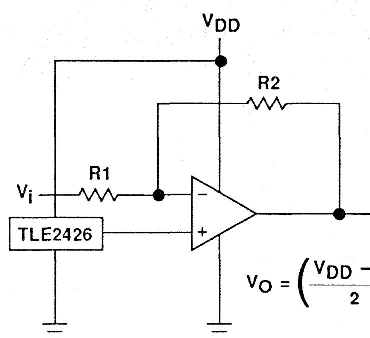
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLV2341 will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.



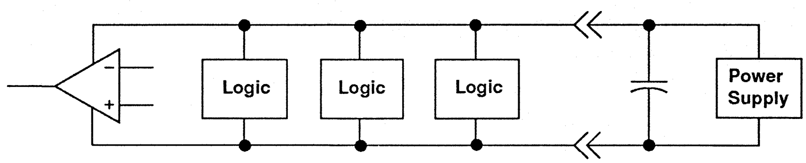
$$V_O = \left(\frac{V_{DD} - V_i}{2}\right)\frac{R_2}{R_1} + \frac{V_{DD}}{2}$$

Figure 97. Inverting Amplifier With Voltage Reference

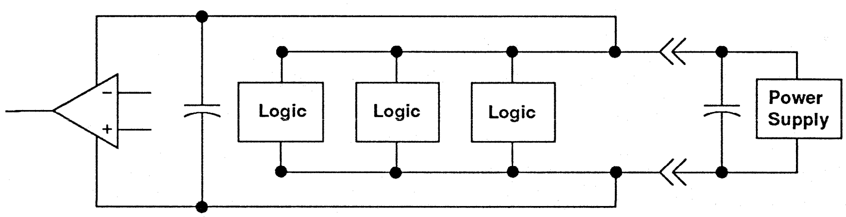
TYPICAL APPLICATION DATA

The TLV2341 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 98); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS

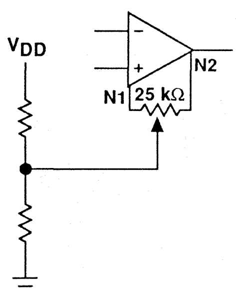


(b) SEPARATE BYPASSED SUPPLY RAILS (preferred)

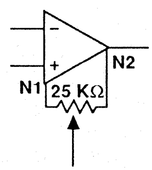
Figure 98. Common Versus Separate Supply Rails

input offset voltage nulling

The TLV2341 offers external input offset null control. Nulling of the input offset voltage may be achieved by adjusting a 25-kΩ potentiometer connected between the offset null terminals with the wiper connected as shown in Figure 99. The amount of nulling range varies with the bias selection. In the high-bias mode, the nulling range will allow the maximum offset voltage specified to be trimmed to zero. In low-bias and medium-bias modes, total nulling may not be possible.



(a) SINGLE-SUPPLY



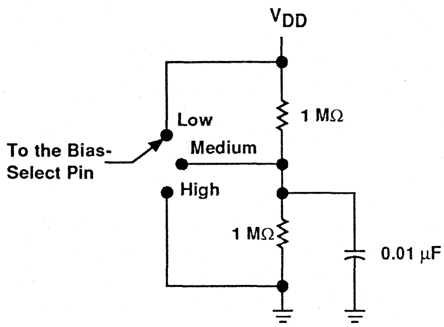
(b) SPLIT-SUPPLY

Figure 99. Input Offset Voltage Null Circuit

TYPICAL APPLICATION DATA

bias selection

Bias selection is achieved by connecting the bias-select pin to one of the three voltage levels (see Figure 100). For medium-bias applications, it is recommended that the bias-select pin be connected to the midpoint between the supply rails. This is a simple procedure in split-supply applications, since this point is ground. In single-supply applications, the medium-bias mode will necessitate using a voltage divider as indicated. The use of large-value resistors in the voltage divider will reduce the current drain of the divider from the supply line. However, large-value resistors used in conjunction with a large-value capacitor will require significant time to charge up to the supply midpoint after the supply is switched on. A voltage other than the midpoint may be used if it is within the voltages specified in the following table.



BIAS MODE	BIAS-SELECT VOLTAGE (Single Supply)
LOW	V_{DD}
MEDIUM	1 V to V_{DD} – 1 V
HIGH	GND

Figure 100. Bias Selection for Single-Supply Applications

input characteristics

The TLV2341 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2341 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low bias current requirements, the TLV2341 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 95 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 101).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

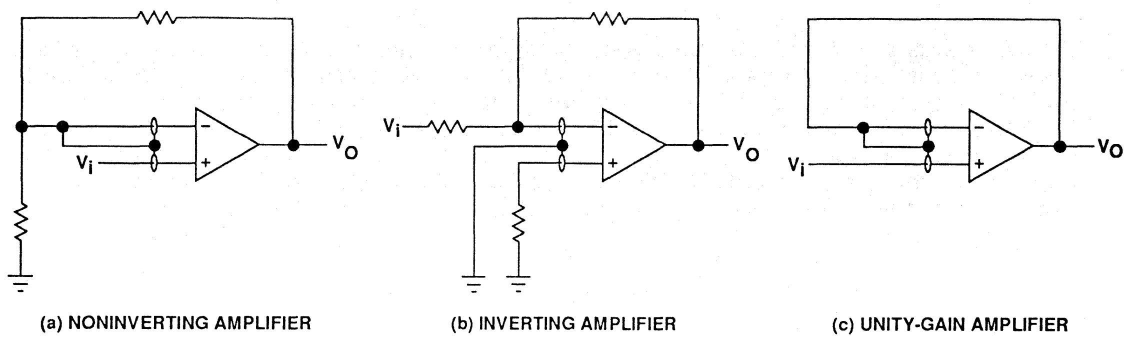


Figure 101. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2341 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 102). The value of this capacitor is optimized empirically.

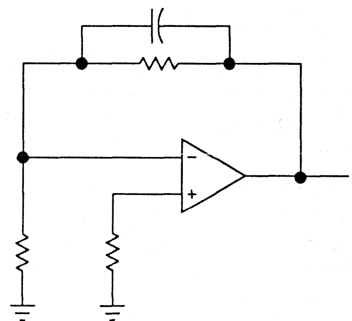


Figure 102. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2341 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2341 inputs and output are designed to withstand –100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

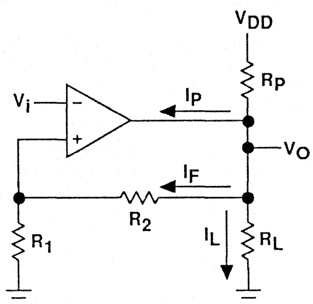
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2341 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2341 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 103). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2341 are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 105, 106, and 107). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 µA)

Figure 103. Resistive Pullup to Increase V_{OH}

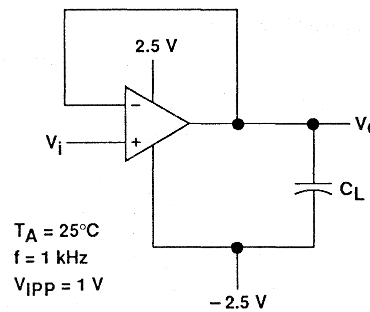
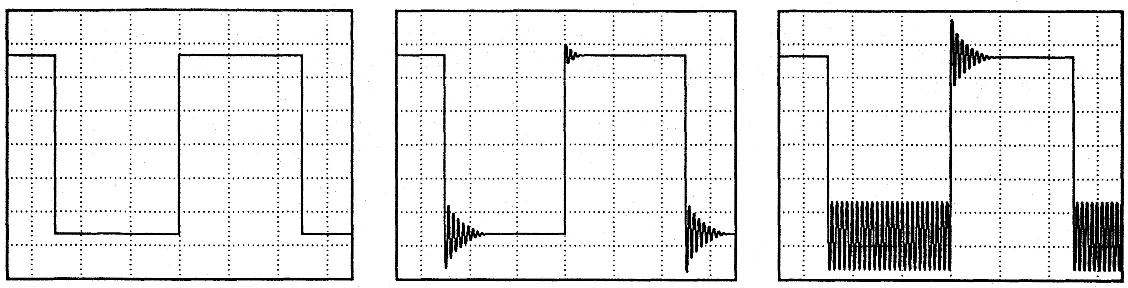


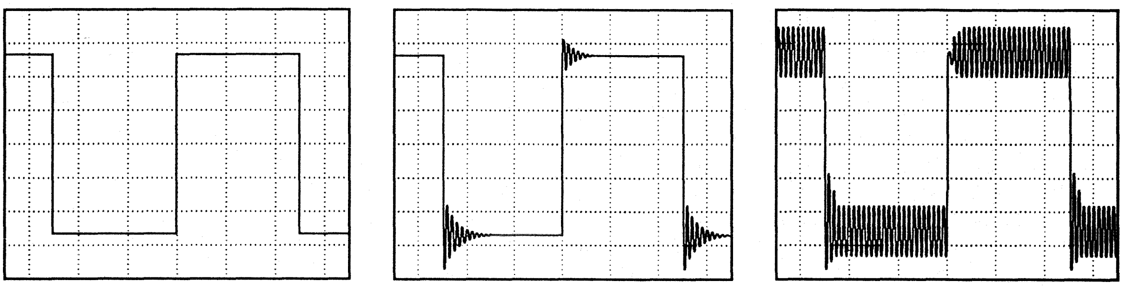
Figure 104. Test Circuit for OutputCharacteristics

TYPICAL APPLICATION DATA



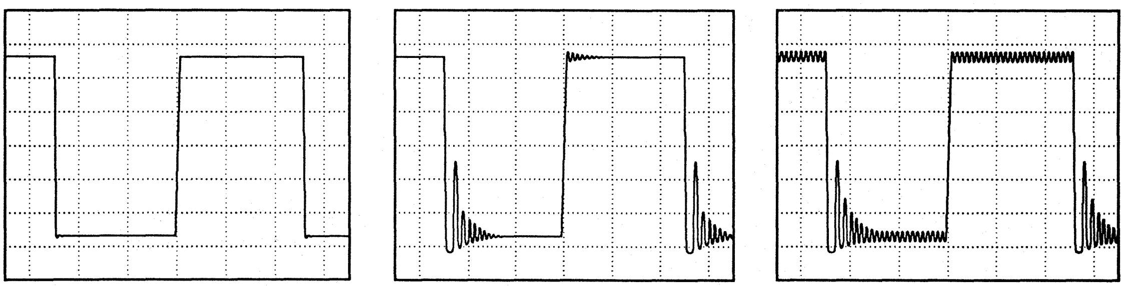
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 105. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 106. Effect of Capacitive Loads in Medium-Bias Mode

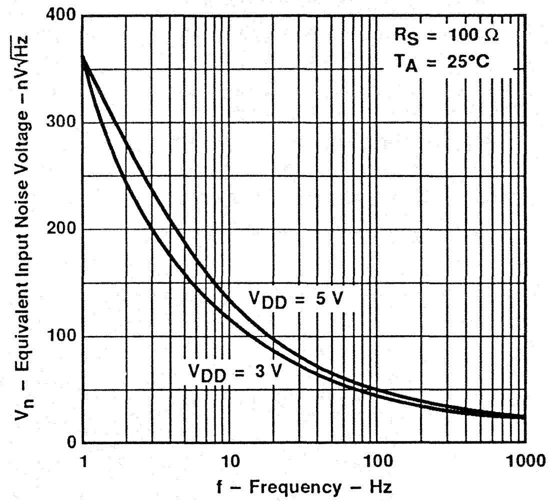


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

Figure 107. Effect of Capacitive Loads in Low-Bias Mode

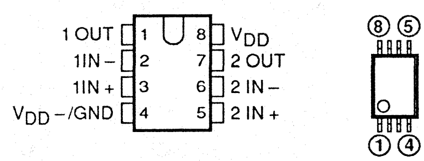
- Wide Range of Supply Voltages Over Specified Temperature Range:
  – 40°C to 85°C . . . 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} – 1 V at 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Designed-In Latchup Immunity

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY



D OR P PACKAGE
(TOP VIEW)

PW PACKAGE
(TOP VIEW)



description

The TLV2342 dual operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2342 was developed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2342 has a typical slew rate of 2.1 V/µs and 790 kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V, and is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of – 40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

Low-voltage and low-power operation has been made possible by using Texas Instruments silicon gate LinCMOS™ technology. The LinCMOS process also features extremely-high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2342 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

To facilitate the design of small portable equipment, the TLV2342 is made availabe in a wide range of package options, including the small-outline and thin-scaled-small-outline packages (TSSOP).The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
– 40°C to 85°C	9 mV	TLV2342ID	TLV2342IP	TLV2342IPW	TLV2342Y

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLV2342IDR).
The PW package is only available left-end taped and reeled (e.g., TLV2342IPWLE).

LinCMOS™ is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

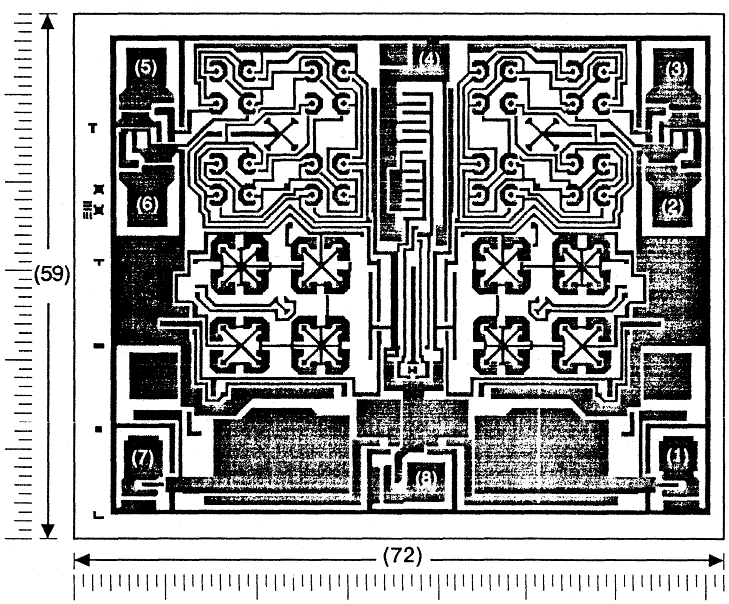
description (continued)

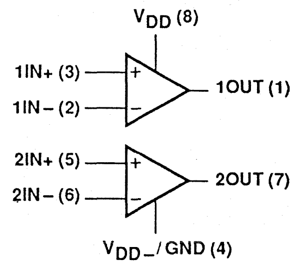
The device inputs and outputs are designed to withstand –100-mA currents without sustaining latch-up. The TLV2342 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

TLV2342Y chip information

These chips, properly assembled, display characteristics similar to the TLV2342I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

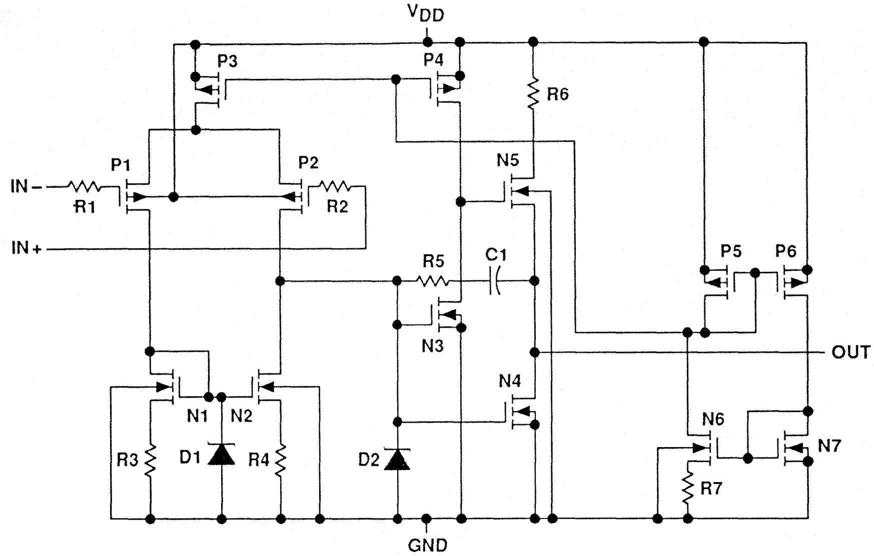
TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)

COMPONENT COUNT†	
Transistors	54
Diodes	4
Resistors	14
Capacitors	2

†Includes both amplifiers and all ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{DD} (see Note 1) . . . 8 V
Differential input voltage (see Note 2) . . . ± V_{DD}
Input voltage range, V_I (any input) . . . – 0.3 V to V_{DD}
Input current, I_I . . . ± 5 mA
Output current, I_O . . . ± 30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . Unlimited
Continuous total dissipation . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . – 40°C to 85°C
Storage temperature range . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package . . . 260°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	– 0.2	1.8	V
	$V_{DD} = 5$ V	– 0.2	3.8	
Operating free-air temperature, T_A		– 40	85	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		0.6	9		1.1	9	mV
			Full range			11			11	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	− 0.2 to 2	− 0.3 to 2.3		− 0.2 to 4	− 0.3 to 4.2		V
			Full range	− 0.2 to 1.8			− 0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V V_{IC} = 1 V, No load	25°C		0.65	3		1.4	3.2	mA
			Full range			4			4.4	

†Full range is – 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		2.1		V/µs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 30		25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 10 kΩ, See Figure 32		25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 10 kΩ See Figure 32		−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		3.6		V/µs
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 92		25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 10 kΩ, See Figure 32		25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 10 kΩ, See Figure 32		−40°C		49°		
				25°C		46°		
				85°C		43°		

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		0.6	9		1.1	9	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	95		70	95		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		0.65	3		1.4	3.2	mA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Gain-bandwidth product	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE

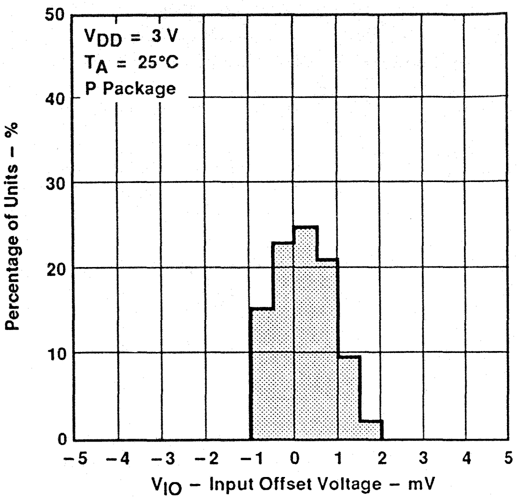


Figure 1

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE

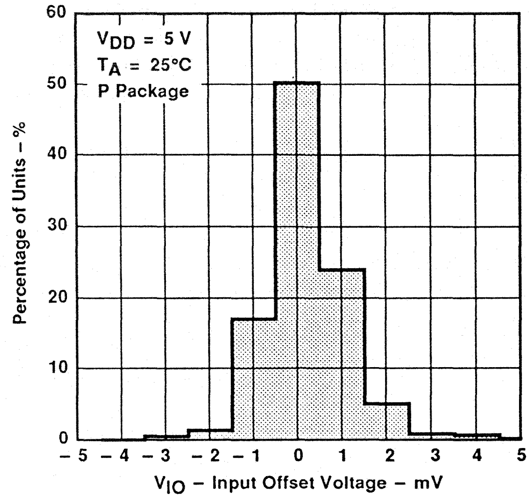


Figure 2

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

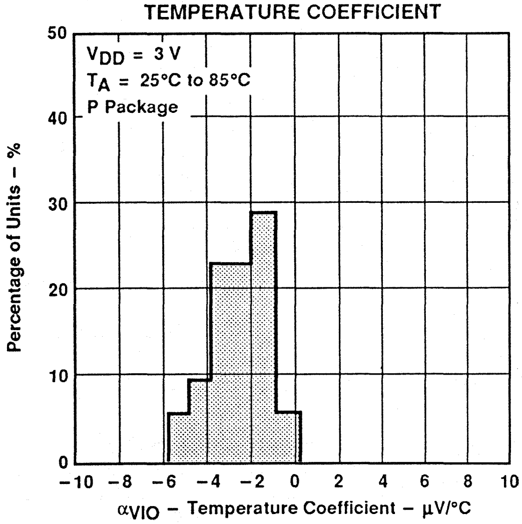


Figure 3

DISTRIBUTION OF TLV2342
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

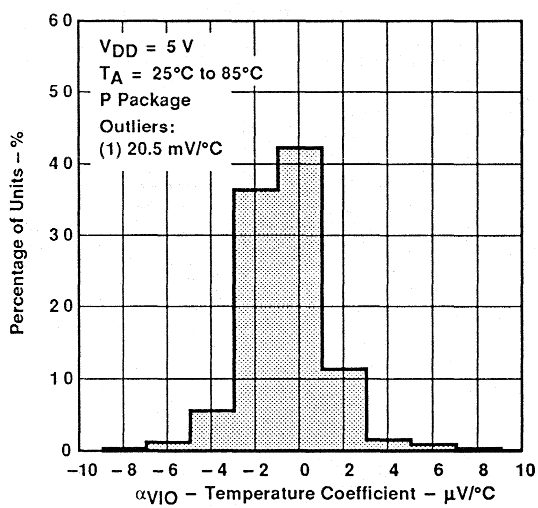


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

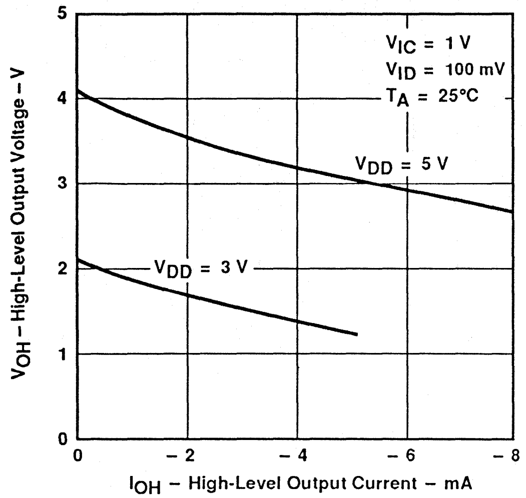


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE vs SUPPLY VOLTAGE

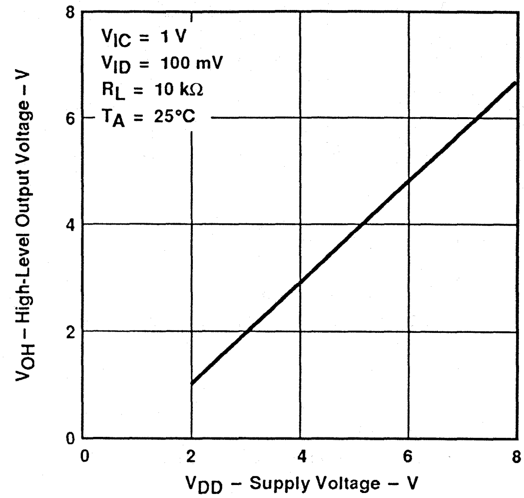


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

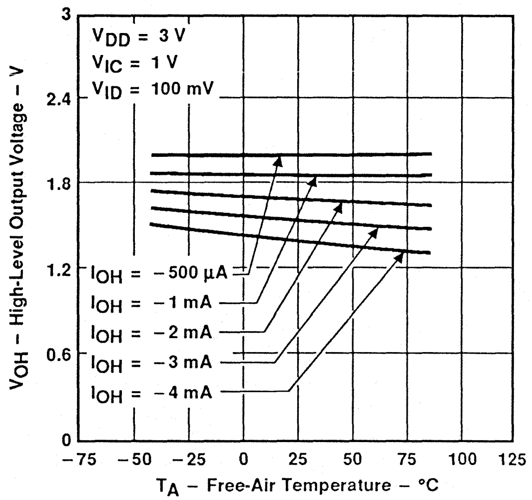


Figure 7

LOW-LEVEL OUTPUT VOLTAGE vs COMMON-MODE INPUT VOLTAGE

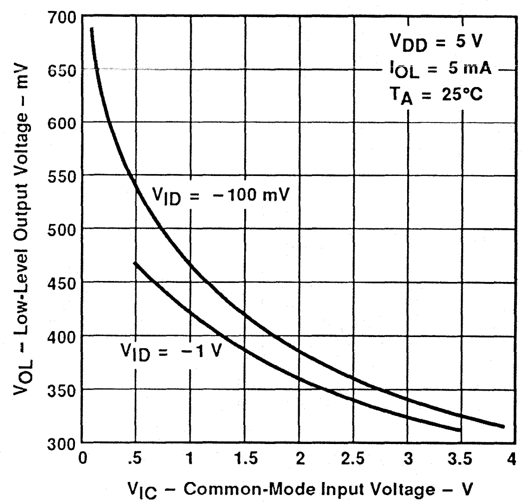


Figure 8

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

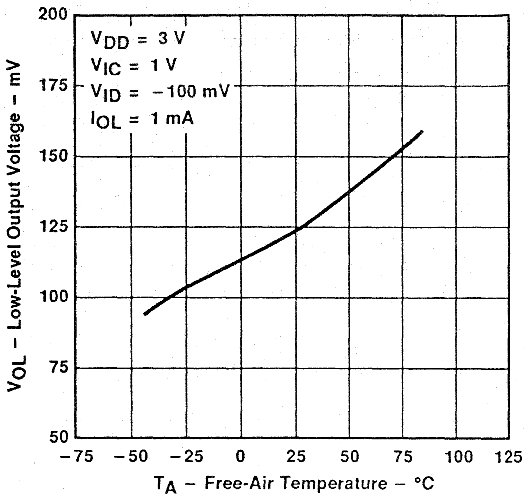


Figure 9

LOW-LEVEL OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

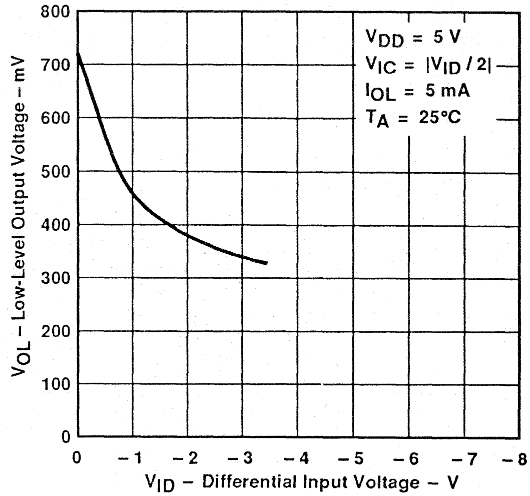


Figure 10

LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

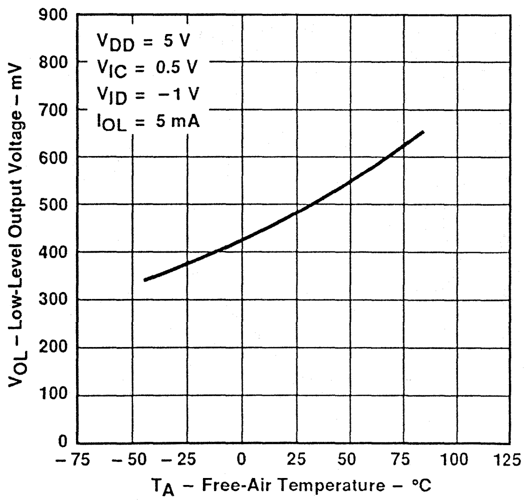


Figure 11

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

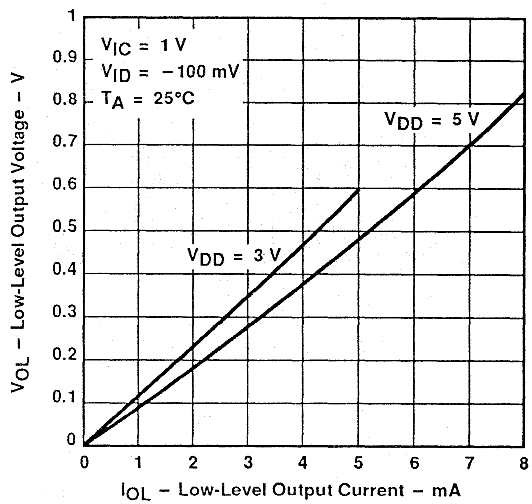


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs SUPPLY VOLTAGE

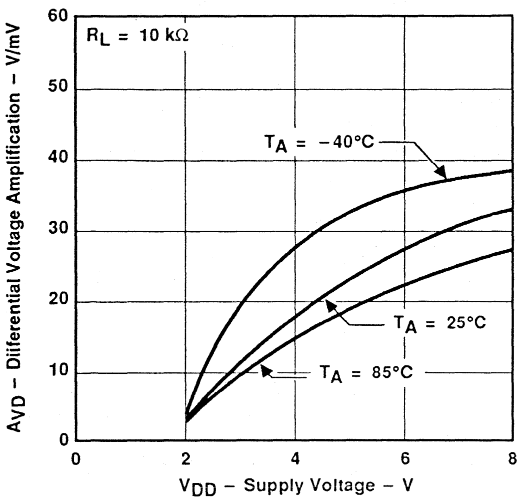


Figure 13

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION vs FREE-AIR TEMPERATURE

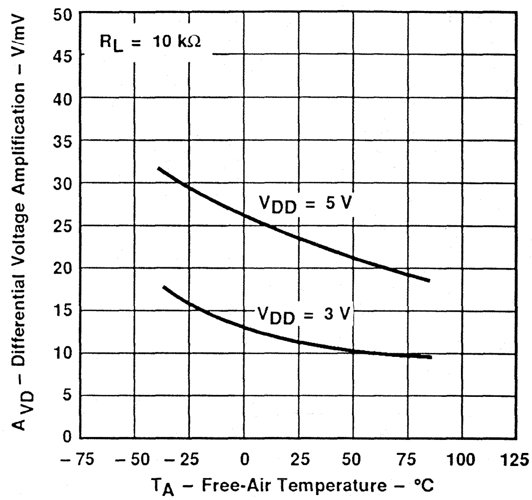


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET CURRENT vs FREE-AIR TEMPERATURE

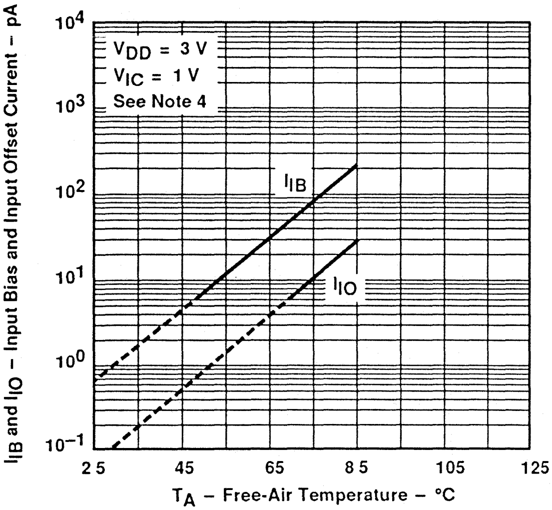


Figure 15

COMMON-MODE INPUT VOLTAGE POSITIVE LIMIT vs SUPPLY VOLTAGE

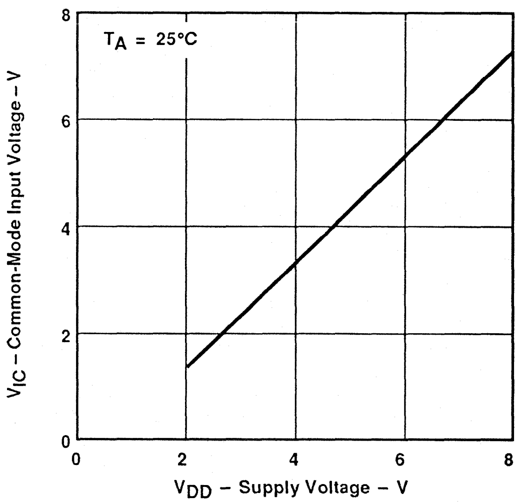


Figure 16

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

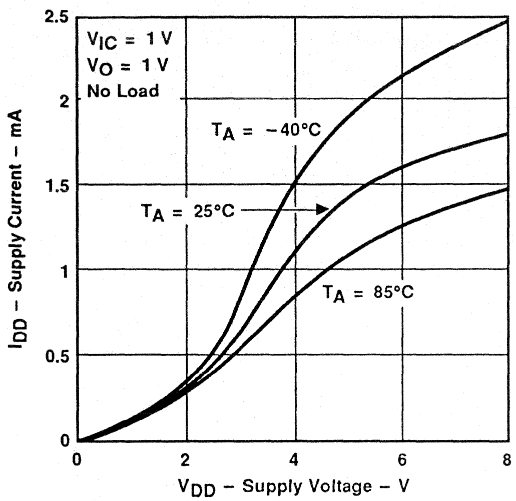


Figure 17

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

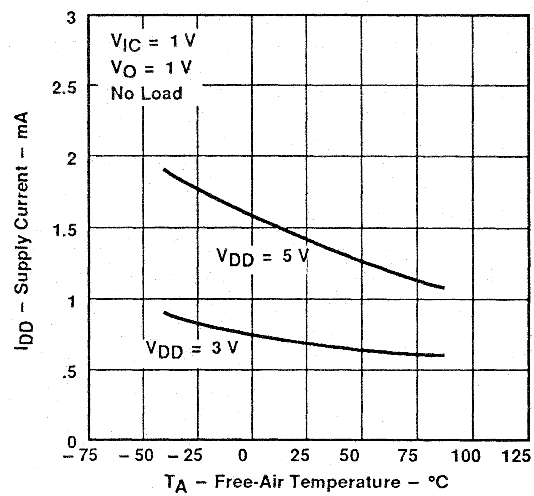


Figure 18

SLEW RATE vs SUPPLY VOLTAGE

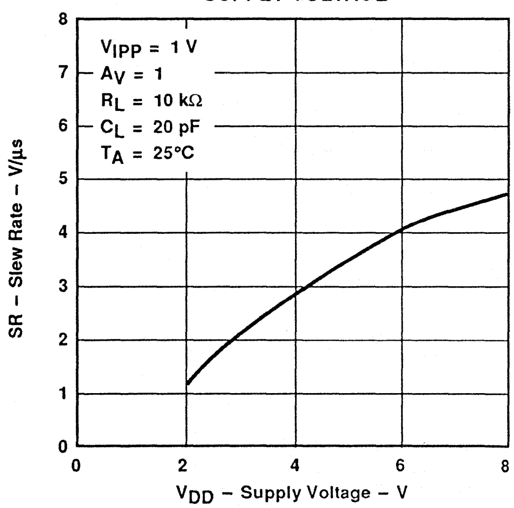


Figure 19

SLEW RATE vs FREE-AIR TEMPERATURE

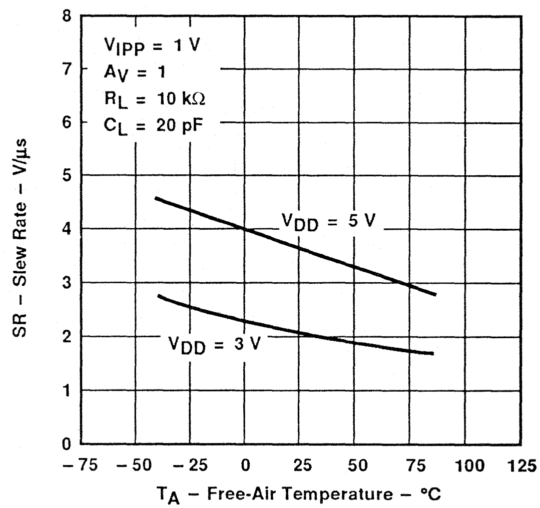


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs FREQUENCY

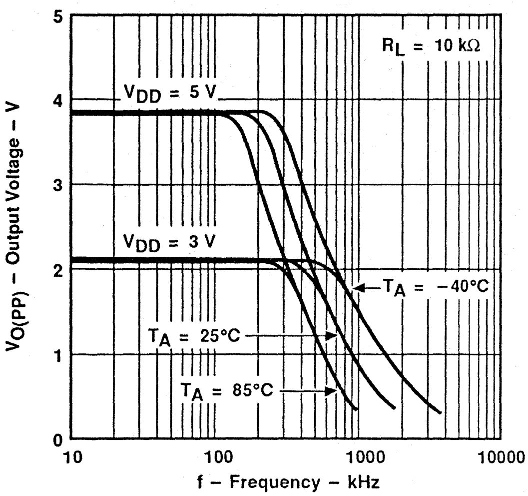


Figure 21

UNITY-GAIN BANDWIDTH vs FREE-AIR TEMPERATURE

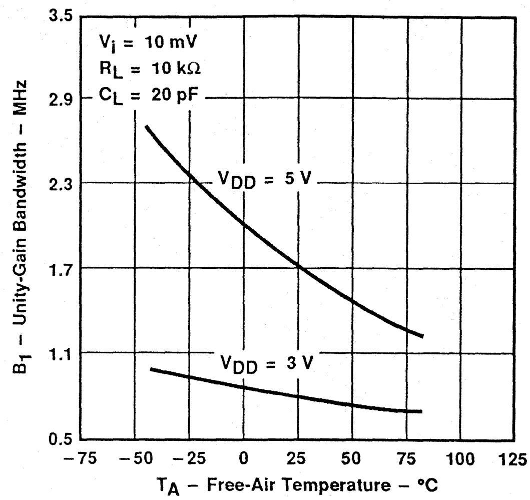


Figure 22

UNITY-GAIN BANDWIDTH vs SUPPLY VOLTAGE

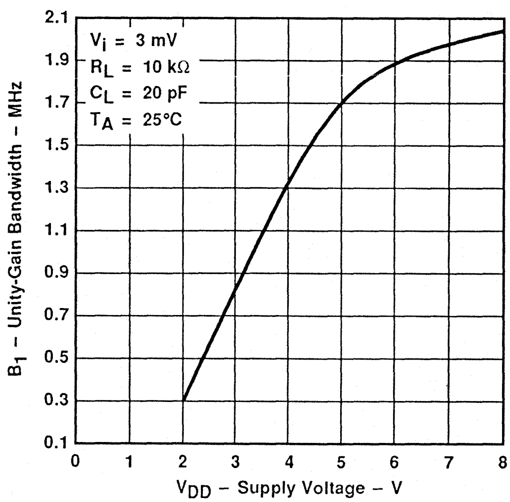


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

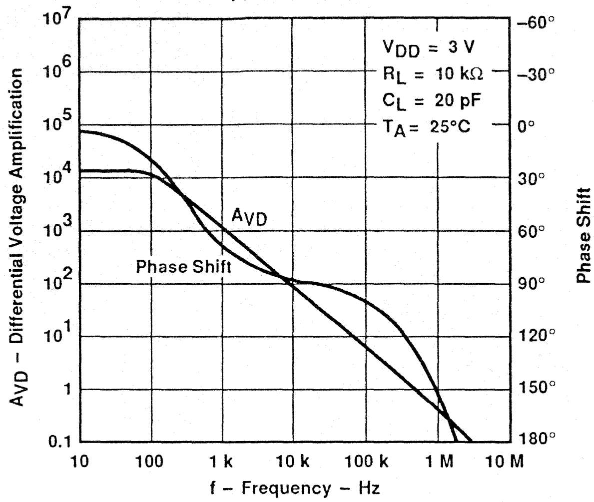


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT vs FREQUENCY

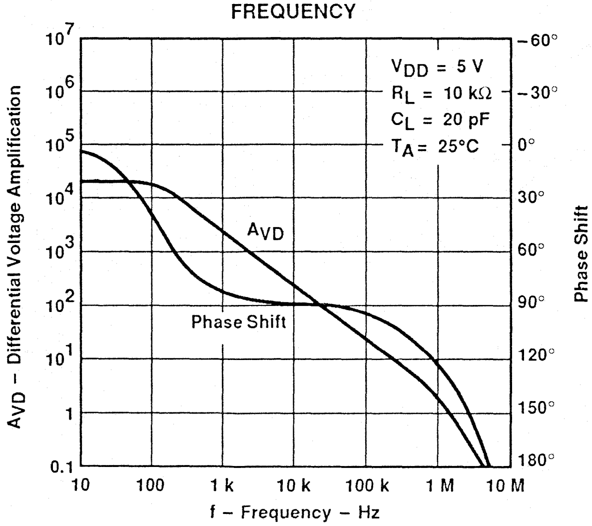


Figure 25

TYPICAL CHARACTERISTICS

PHASE MARGIN vs SUPPLY VOLTAGE

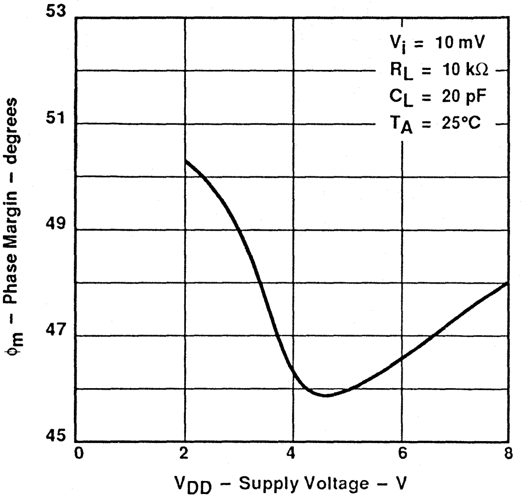


Figure 26

PHASE MARGIN vs FREE-AIR TEMPERATURE

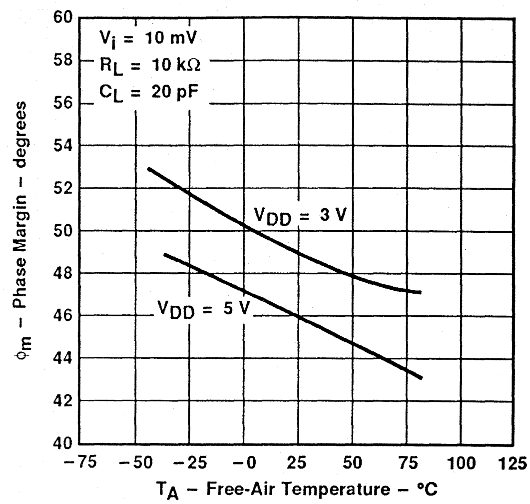


Figure 27

PHASE MARGIN vs LOAD CAPACITANCE

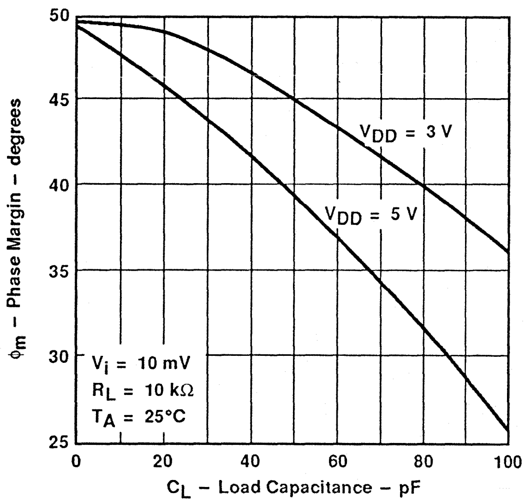


Figure 28

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

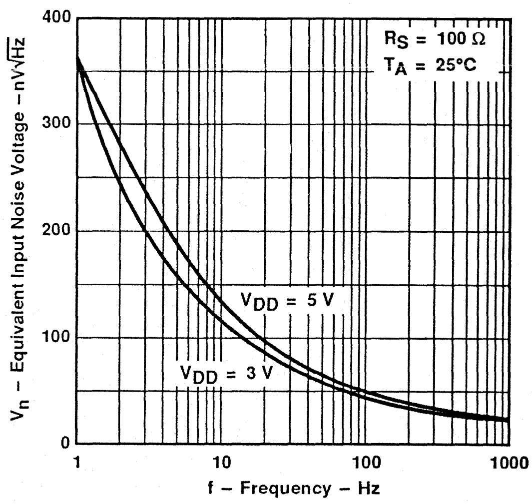
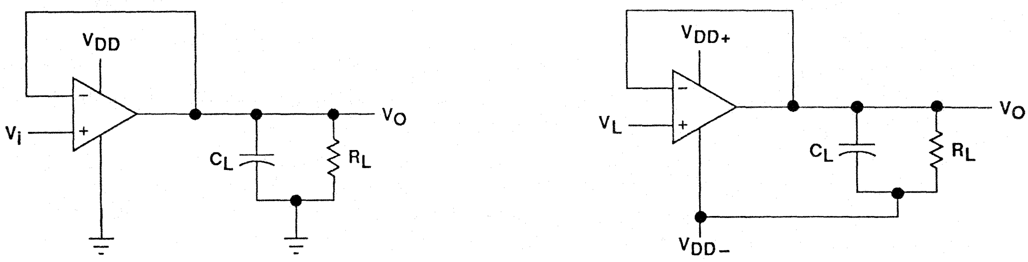


Figure 29

PARAMETER MEASUREMENT INFORMATION

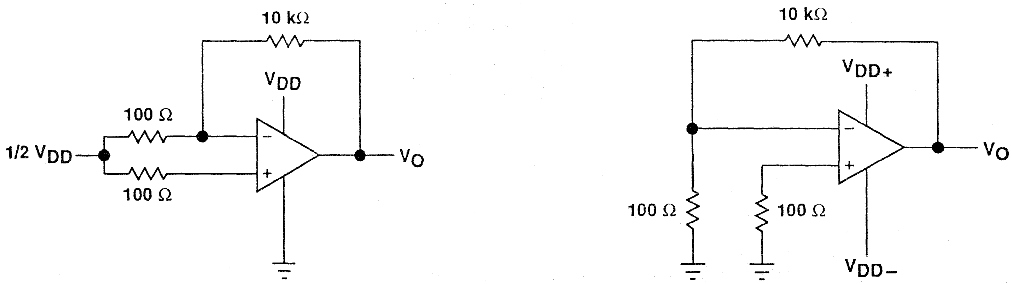
single-supply versus split-supply test circuits

Because the TLV2342 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



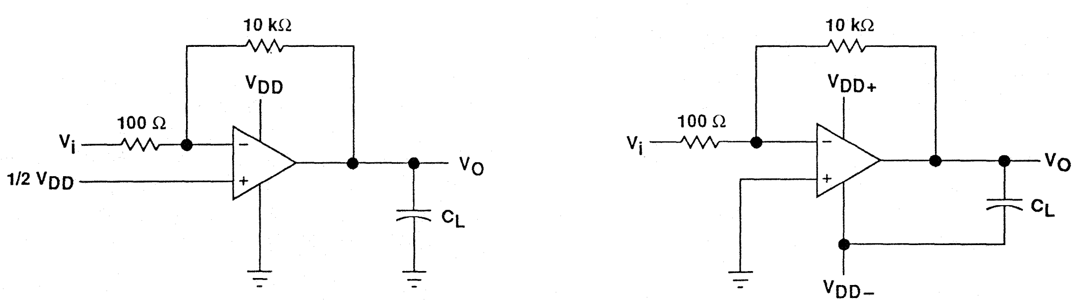
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2342 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

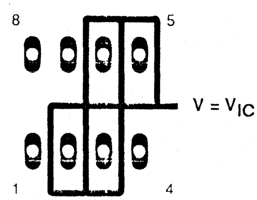


Figure 33. Isolation Metal Around Device Inputs
(P Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

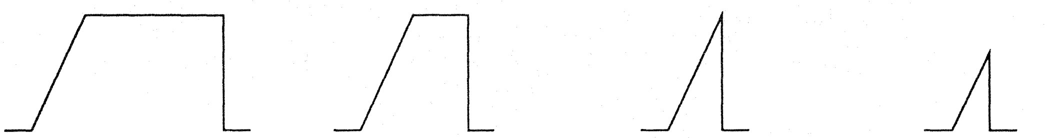
full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 34. Full-Power-Response Output Signal

test time

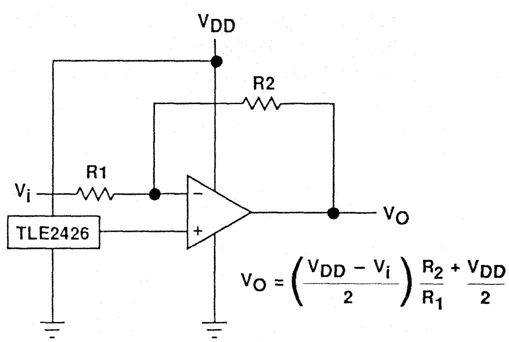
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLV2342 will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.



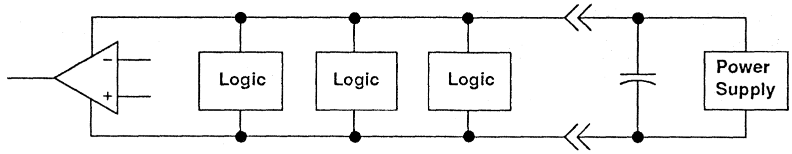
$$V_O = \left(\frac{V_{DD} - V_i}{2}\right)\frac{R_2}{R_1} + \frac{V_{DD}}{2}$$

Figure 35. Inverting Amplifier With Voltage Reference

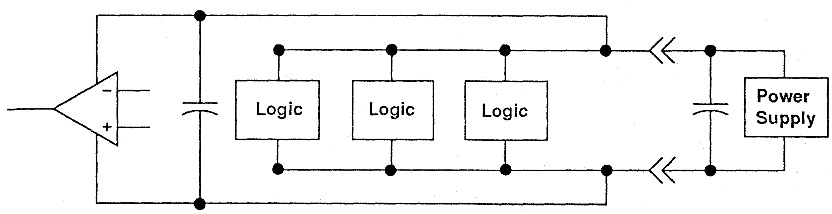
TYPICAL APPLICATION DATA

The TLV2342 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2342 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at V_{DD} – 1 V at T_A = 25°C and at V_{DD} – 1.2 V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2342 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 µV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLV2342 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

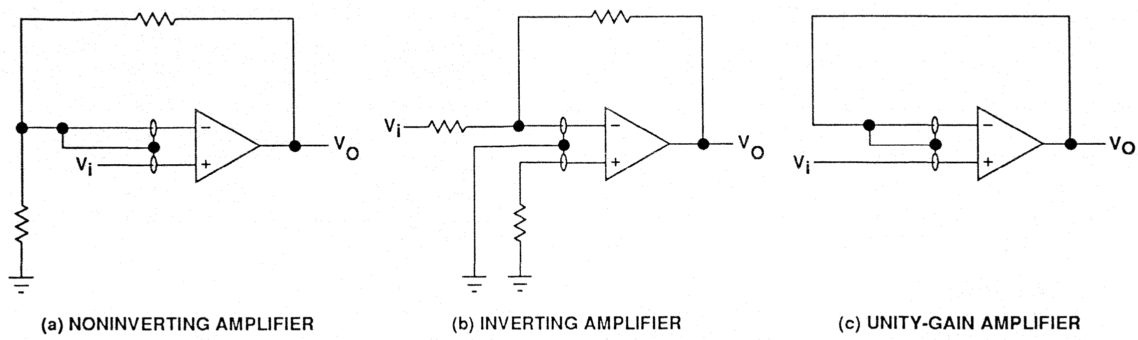


Figure 37. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low-input bias current requirements of the TLV2342 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

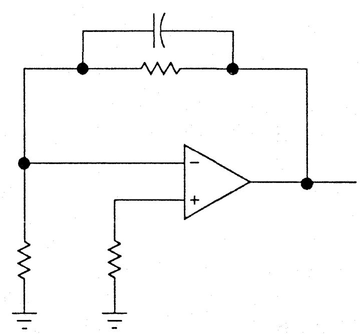


Figure 38. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2342 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2342 inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 μF typical) located across the supply rails as close to the device as possible.

The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2342 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2342 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2342 are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 41, 42, and 43). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.

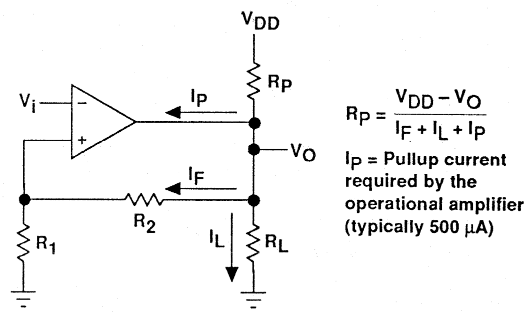


Figure 39. Resistive Pullup to Increase V_{OH}

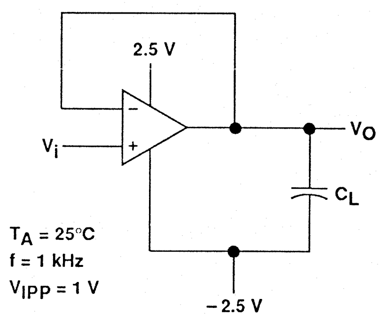
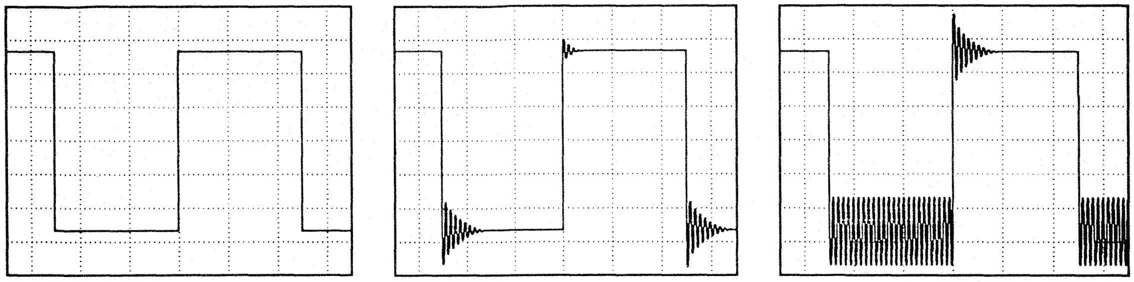


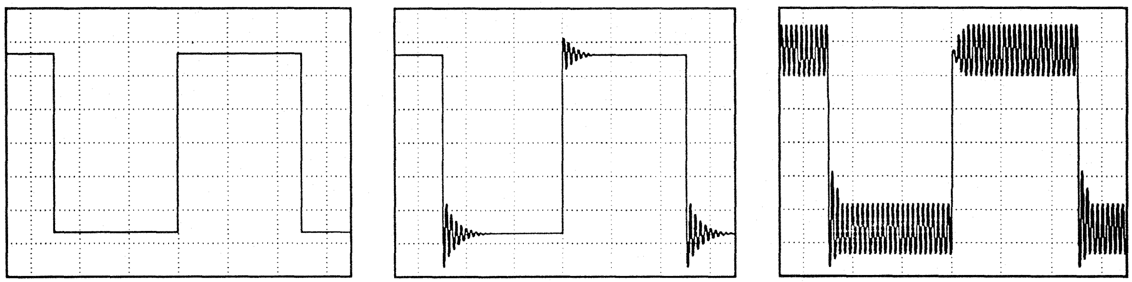
Figure 40. Test Circuit for Output Characteristics

TYPICAL APPLICATION DATA



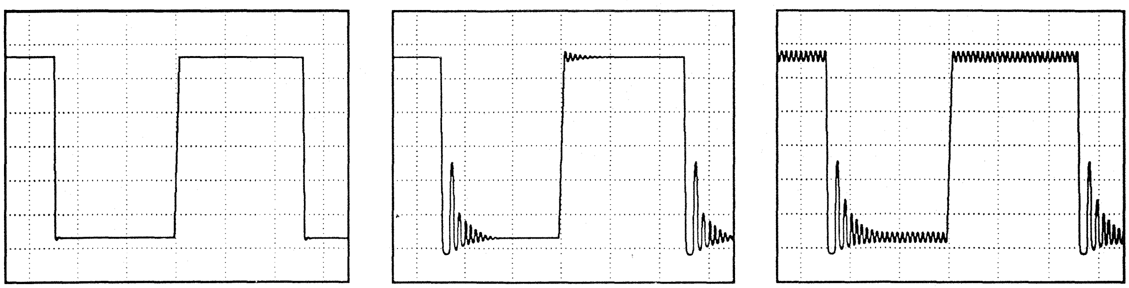
(a) C_L = 20 pF, R_L = NO LOAD   (b) C_L = 130 pF, R_L = NO LOAD   (c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD   (b) C_L = 170 pF, R_L = NO LOAD   (c) C_L = 190 pF, R_L = NO LOAD

Figure 42. Effect of Capacitive Loads in Medium-Bias Mode

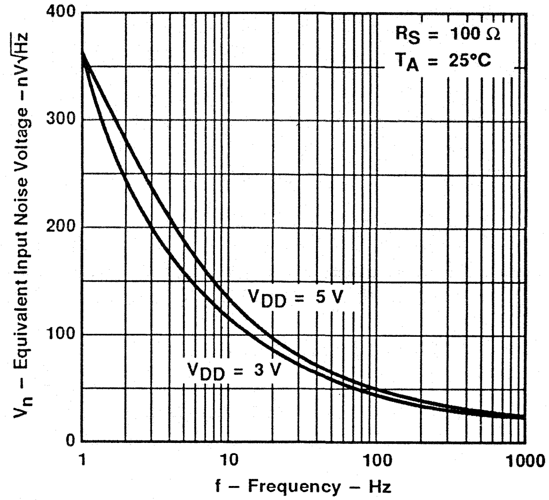


(a) C_L = 20 pF, R_L = NO LOAD   (b) C_L = 260 pF, R_L = NO LOAD   (c) C_L = 310 pF, R_L = NO LOAD

Figure 43. Effect of Capacitive Loads in Low-Bias Mode

- Wide Range of Supply Voltages Over Specified Temperature Range: – 40°C to 85°C . . . 2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Single-Supply Operation
- Common-Mode Input-Voltage Range Extends Below the Negative Rail and up to V_{DD} – 1 V at 25°C
- Output Voltage Range Includes Negative Rail
- High Input Impedance . . . 10^{12} Ω Typical
- ESD-Protection Circuitry
- Designed-In Latch-Up Immunity

EQUIVALENT INPUT NOISE VOLTAGE
vs
FREQUENCY

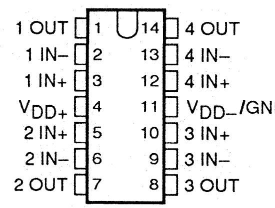


description

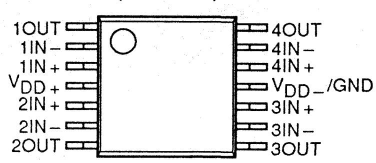
The TLV2344 quad operational amplifier is one of a family of devices that has been specifically designed for use in low-voltage, single-supply applications. Unlike other products in this family designed primarily to meet aggressive power consumption specifications, the TLV2344 is designed to offer ac performance approaching that of a BiFET operational amplifier while operating from a single-supply rail. At 3 V, the TLV2344 has a typical slew rate of 2.1 V/μs and 790-kHz unity-gain bandwidth.

Each amplifier is fully functional down to a minimum supply voltage of 2 V, is fully characterized, tested, and specified at both 3-V and 5-V power supplies over a temperature range of – 40°C to 85°C. The common-mode input voltage range includes the negative rail and extends to within 1 V of the positive rail.

D OR N PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	V_{IO} max AT 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PW)‡	
– 40°C to 85°C	10 mV	TLV2344ID	TLV2344IN	TLV2344IPW	TLV2344Y

†Available in tape-and-reel. Add "R" suffix to the device type when ordering (e.g., TLV2344IDR).
‡The PW packages are only available left-end taped and reeled (e.g., TLV2344IPWLE).

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description (continued)

Low-voltage and low-power operation has been made possible by using Texas Instruments silicon gate LinCMOS™ technology. The LinCMOS process also features extremely high input impedance and ultra-low input bias currents. These parameters combined with good ac performance make the TLV2344 effectual in applications such as high-frequency filters and wide-bandwidth sensors.

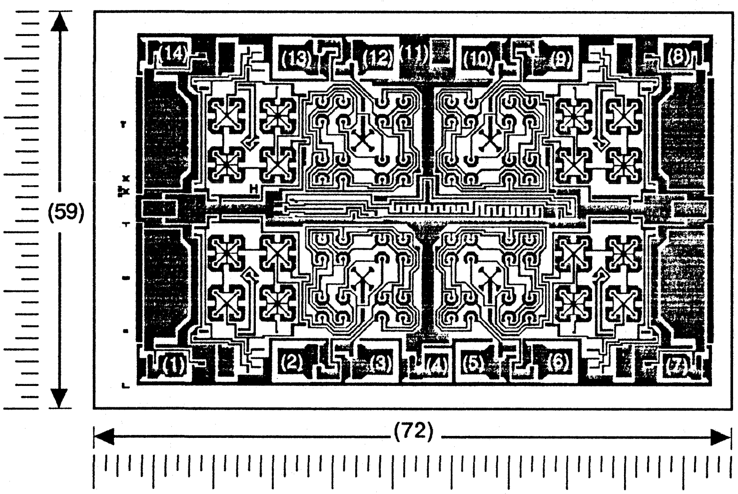
To facilitate the design of small portable equipment, the TLV2344 is made available in a wide range of package options, including the small-outline and thin-scaled-small-outline packages (TSSOP). The TSSOP package has significantly reduced dimensions compared to a standard surface-mount package. Its maximum height of only 1.1 mm makes it particularly attractive when space is critical.

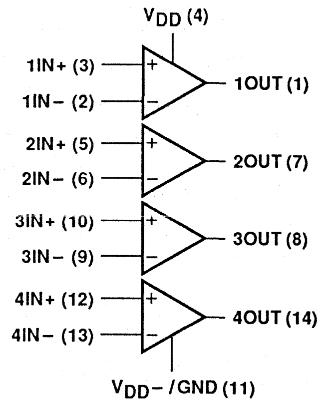
The device inputs and outputs are designed to withstand −100-mA currents without sustaining latch-up. The TLV2344 incorporates internal ESD-protection circuits that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in degradation of the device parametric performance.

TLV2344Y chip information

These chips, properly assembled, display characteristics similar to the TLV2344I (see electrical tables). Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS:
15 TYPICAL

BONDING PADS:
4 X 4 MINIMUM

T_J max = 150°C

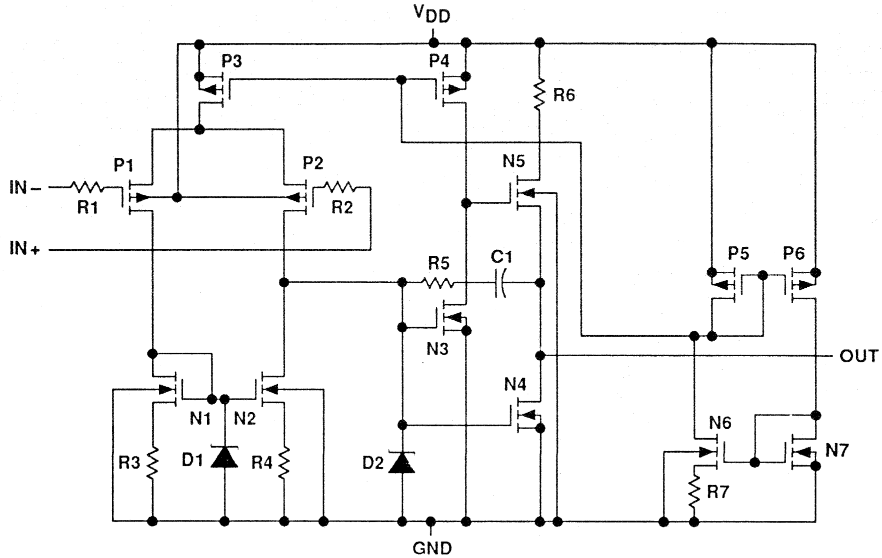
TOLERANCES
ARE ±10%

ALL DIMENSIONS
ARE IN MILS

equivalent schematic (each amplifier)

COMPONENT COUNT†	
Transistors	8
Diodes	28
Resistors	4
Capacitors	108

†Includes both amplifiers and all ESD, bias, and trim circuitry



absolute maximum ratings over operating free-air temperature (unless otherwise noted)‡

Supply voltage, V_{DD} (see Note 1) . . . . . 8 V
Differential input voltage (see Note 2) . . . . . ± V_{DD}
Input voltage range, V_I (any input) . . . . . – 0.3 V to V_{DD}
Input current, I_I . . . . . ± 5 mA
Output current, I_O . . . . . ± 30 mA
Duration of short-circuit current at (or below) T_A = 25°C (see Note 3) . . . . . Unlimited
Continuous total dissipation . . . . . See Dissipation Rating Table
Operating free-air temperature range, T_A . . . . . – 40°C to 85°C
Storage temperature range . . . . . – 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package . . . . . 260°C

‡Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "reccommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input with respect to the inverting input.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1575 mW	5.6 mW/°C	364 mW
PW	700 mW	12.6 mW/°C	819 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	$V_{DD} = 3$ V	– 0.2	1.8	V
	$V_{DD} = 5$ V	– 0.2	3.8	
Operating free-air temperature, T_A		– 40	85	°C

electrical characteristics at specified free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A†	V_{DD} = 3 V MIN	V_{DD} = 3 V TYP	V_{DD} = 3 V MAX	V_{DD} = 5 V MIN	V_{DD} = 5 V TYP	V_{DD} = 5 V MAX	UNIT
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ	25°C		1.1	10		1.1	10	mV
			Full range			12			12	
α_{VIO}	Average temperature coefficient of input offset voltage		25°C to 85°C		2.7			2.7		μV/°C
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.1			0.1		pA
			85°C		22	1000		24	1000	
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V	25°C		0.6			0.6		pA
			85°C		175	2000		200	2000	
V_{ICR}	Common-mode input voltage range (see Note 5)		25°C	−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
			Full range	−0.2 to 1.8			−0.2 to 3.8			V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	25°C	1.75	1.9		3.2	3.7		V
			Full range	1.7			3			
V_{OL}	Low-level output voltage	V_{IC} = 1 V V_{ID} = − 100 mV, I_{OL} = 1 mA	25°C		120	150		90	150	mV
			Full range			190			190	
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	25°C	3	11		5	23		V/mV
			Full range	2			3.5			
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	25°C	65	78		65	80		dB
			Full range	60			60			
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	25°C	70	95		70	95		dB
			Full range	65			65			
I_{DD}	Supply current	V_O = 1 V V_{IC} = 1 V, No load	25°C		1.3	6		2.7	6.4	mA
			Full range			8			8.8	

†Full range is − 40°C to 85°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

operating characteristics at specified free-air temperature, V_{DD} = 3 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		2.1		V/μs
				85°C		1.7		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 30		25°C		170		kHz
				85°C		145		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 10 kΩ, See Figure 32		25°C		790		kHz
				85°C		690		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 10 kΩ See Figure 32		−40°C		53°		
				25°C		49°		
				85°C		47°		

operating characteristics at specified free-air temperature, V_{DD} = 5 V

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_{IC} = 1 V, R_L = 10 kΩ, C_L = 20 pF, See Figure 30	V_{IPP} = 1 V	25°C		3.6		V/μs
				85°C		2.8		
			V_{IPP} = 2.5 V	25°C		2.9		
				85°C		2.3		
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω, See Figure 31		25°C		25		nV/√Hz
B_{OM}	Maximum output swing bandwidth	V_O = V_{OH}, C_L = 20 pF, R_L = 10 kΩ, See Figure 92		25°C		320		kHz
				85°C		250		
B_1	Unity-gain bandwidth	V_i = 10 mV, C_L = 20 pF, R_L = 10 kΩ, See Figure 32		25°C		1.7		MHz
				85°C		1.2		
ϕ_m	Phase margin	V_i = 10 mV, f = B_1, C_L = 20 pF, R_L = 10 kΩ, See Figure 32		−40°C		49°		
				25°C		46°		
				85°C		43°		

electrical characteristics at specified free-air temperature, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	V_O = 1 V, V_{IC} = 1 V, R_S = 50 Ω, R_L = 10 kΩ		1.1	10		1.1	10	mV
I_{IO}	Input offset current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.1			0.1		pA
I_{IB}	Input bias current (see Note 4)	V_O = 1 V, V_{IC} = 1 V		0.6			0.6		pA
V_{ICR}	Common-mode input voltage range (see Note 5)		−0.2 to 2	−0.3 to 2.3		−0.2 to 4	−0.3 to 4.2		V
V_{OH}	High-level output voltage	V_{IC} = 1 V, V_{ID} = 100 mV, I_{OL} = −1 mA	1.75	1.9		3.2	3.7		V
V_{OL}	Low-level output voltage	V_{IC} = 1 V, V_{ID} = −100 mV, I_{OL} = 1 mA		120	150		90	150	mV
A_{VD}	Large-signal differential voltage amplification	V_{IC} = 1 V, R_L = 10 kΩ, See Note 6	3	11		5	23		V/mV
CMRR	Common-mode rejection ratio	V_O = 1 V, V_{IC} = V_{ICR}min, R_S = 50 Ω	65	78		65	80		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD} / \Delta V_{IO}$)	V_{DD} = 3 V to 5 V, V_{IC} = 1 V, V_O = 1 V, R_S = 50 Ω	70	95		70	95		dB
I_{DD}	Supply current	V_O = 1 V, V_{IC} = 1 V, No load		1.3	6		2.7	6.4	μA

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.
6. At V_{DD} = 5 V, V_O = 0.25 V to 2 V; at V_{DD} = 3 V, V_O = 0.5 V to 1.5 V.

TYPICAL CHARACTERISTICS

			FIGURE
V_{IO}	Input offset voltage	Distribution	1, 2
α_{VIO}	Input offset voltage temperature coefficient	Distribution	3, 4
V_{OH}	High-level output voltage	vs Output current	5
		vs Supply voltage	6
		vs Temperature	7
V_{OL}	Low-level output voltage	vs Common-mode input voltage	8
		vs Temperature	9, 11
		vs Differential input voltage	10
		vs Low-level output current	12
A_{VD}	Differential voltage amplification	vs Supply voltage	13
		vs Temperature	14
I_{IB}/I_{IO}	Input bias and offset current	vs Temperature	15
V_{IC}	Common-mode input voltage	vs Supply voltage	16
I_{DD}	Supply current	vs Supply voltage	17
		vs Temperature	18
SR	Slew rate	vs Supply voltage	19
		vs Temperature	20
$V_{(OPP)}$	Maximum peak-to-peak output voltage	vs Frequency	21
B_1	Gain-bandwidth product	vs Temperature	22
		vs Supply voltage	23
A_{VD}	Differential voltage amplification and phase shift	vs Frequency	24, 25
ϕ_m	Phase margin	vs Supply voltage	26
		vs Temperature	27
		vs Load capacitance	28
V_n	Equivalent input noise voltage	vs Frequency	29

TYPICAL CHARACTERISTICS

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE

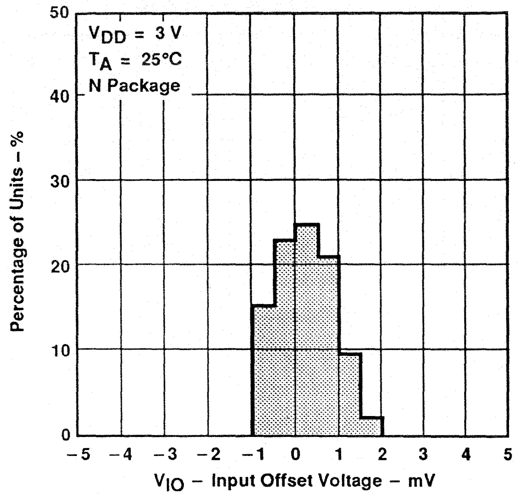


Figure 1

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE

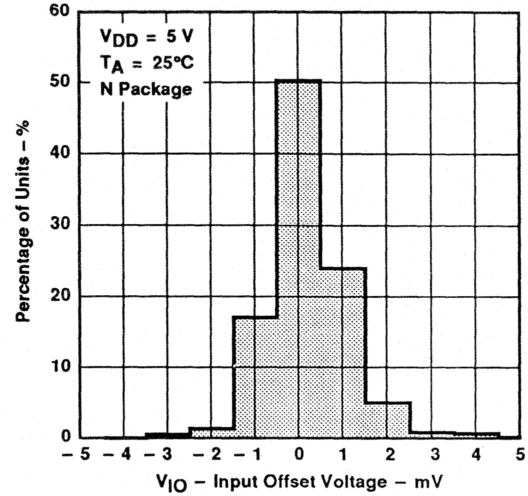


Figure 2

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

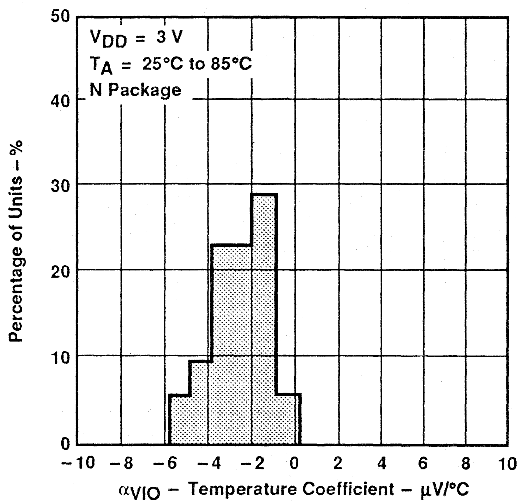


Figure 3

DISTRIBUTION OF TLV2344
INPUT OFFSET VOLTAGE
TEMPERATURE COEFFICIENT

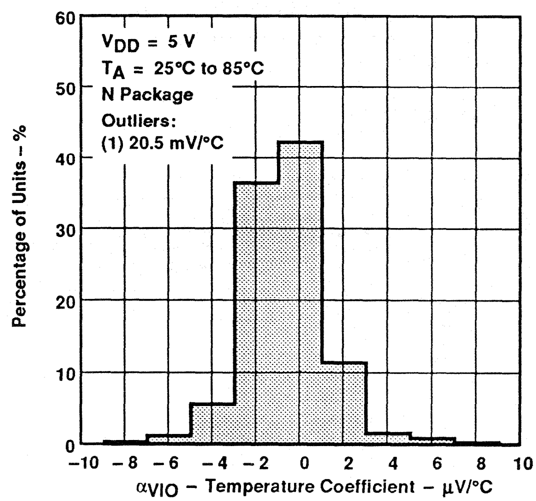


Figure 4

TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

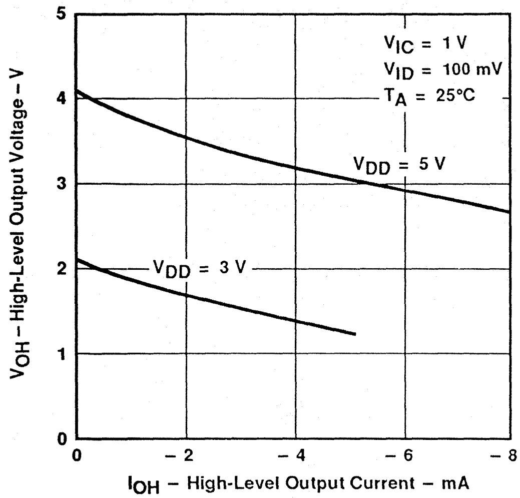


Figure 5

HIGH-LEVEL OUTPUT VOLTAGE
vs
SUPPLY VOLTAGE

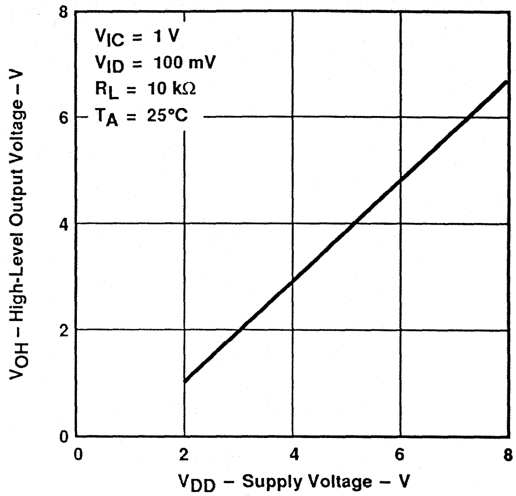


Figure 6

HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

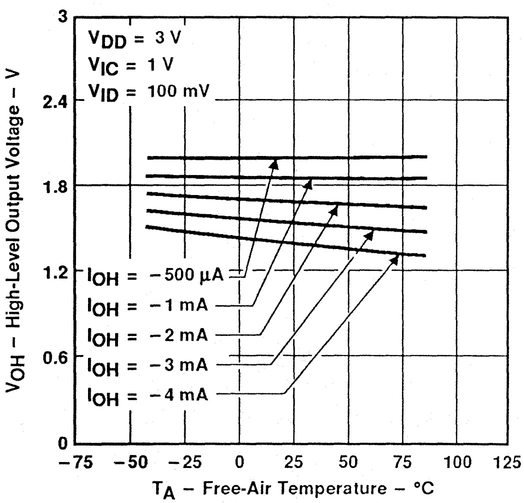


Figure 7

LOW-LEVEL OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

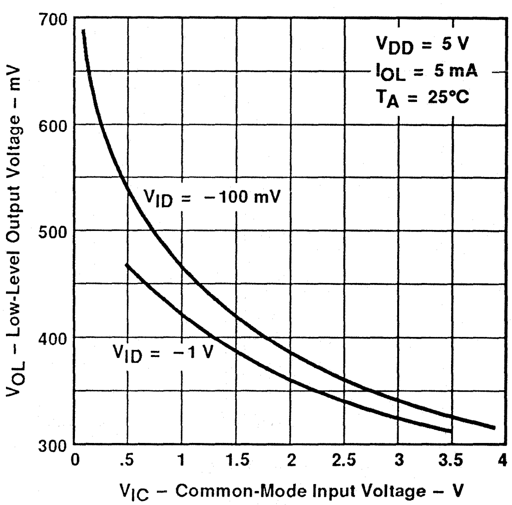


Figure 8

TYPICAL CHARACTERISTICS

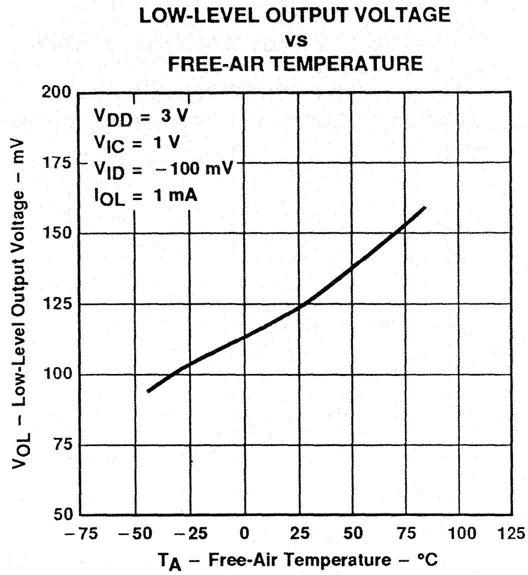


Figure 9

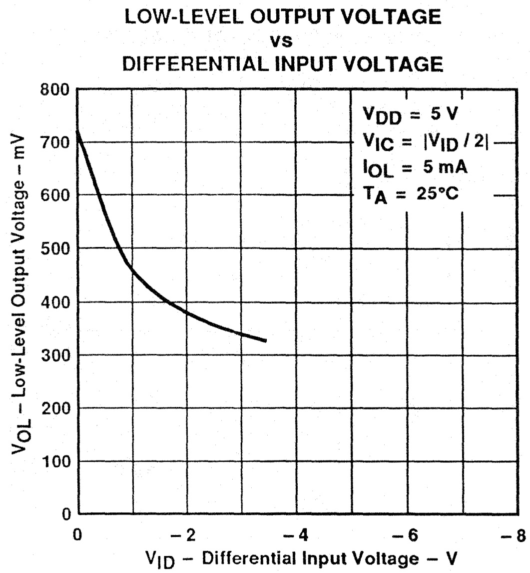


Figure 10

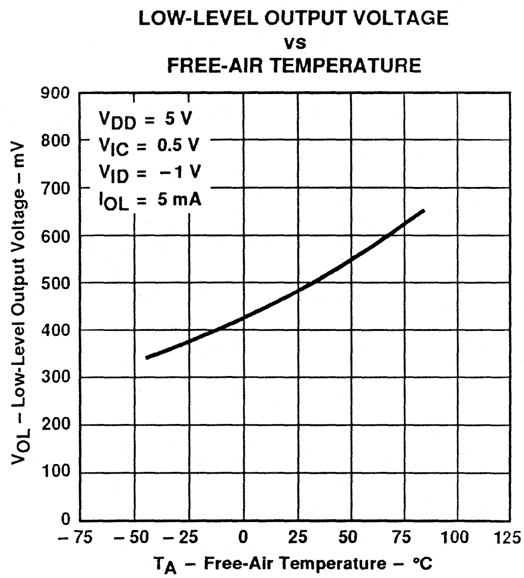


Figure 11

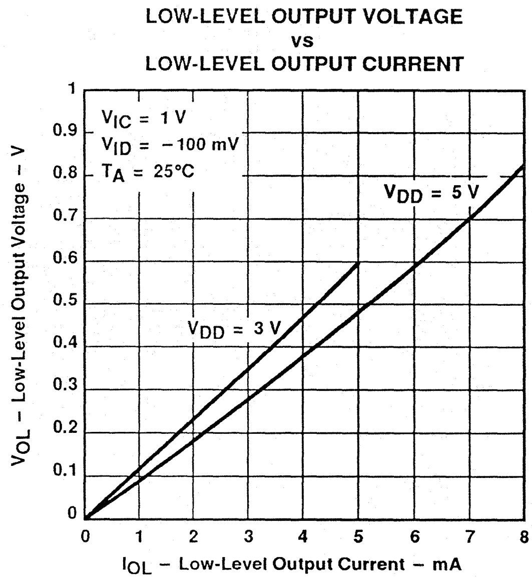


Figure 12

TYPICAL CHARACTERISTICS

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
SUPPLY VOLTAGE

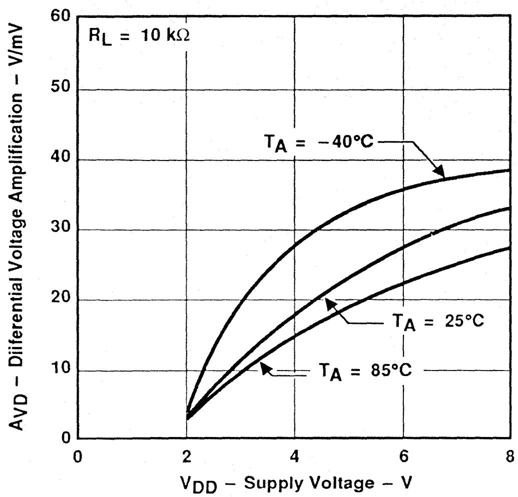


Figure 13

LARGE-SIGNAL
DIFFERENTIAL VOLTAGE AMPLIFICATION
vs
FREE-AIR TEMPERATURE

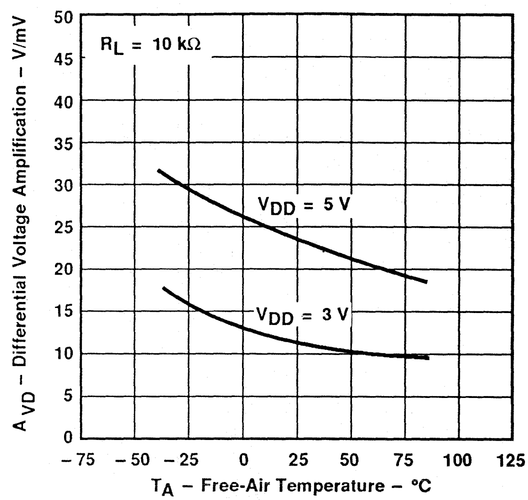


Figure 14

INPUT BIAS CURRENT AND INPUT OFFSET
CURRENT
vs
FREE-AIR TEMPERATURE

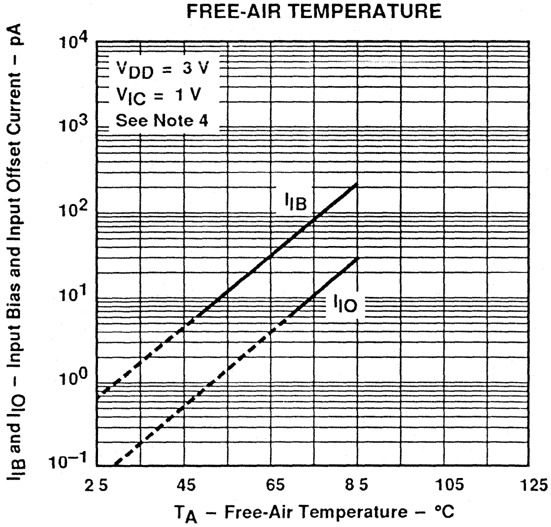


Figure 15

COMMON-MODE INPUT VOLTAGE
POSITIVE LIMIT
vs
SUPPLY VOLTAGE

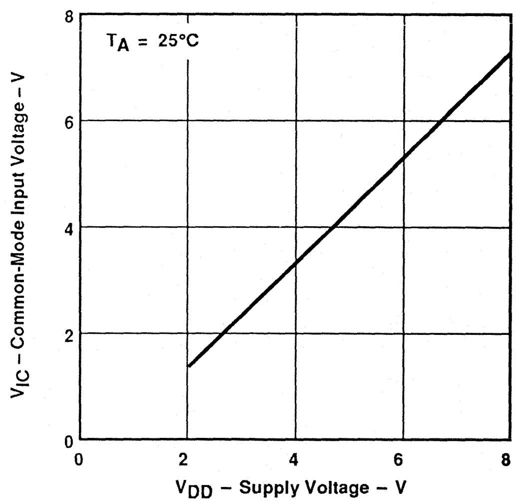


Figure 16

NOTE 4: The typical values of input bias current and input offset current below 5 pA were determined mathematically.

TYPICAL CHARACTERISTICS

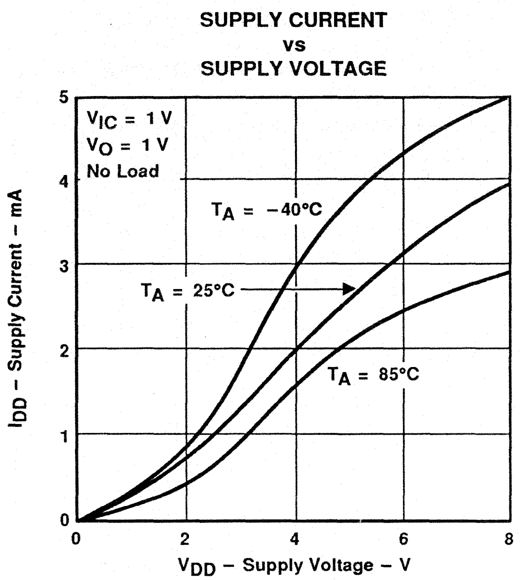


Figure 17

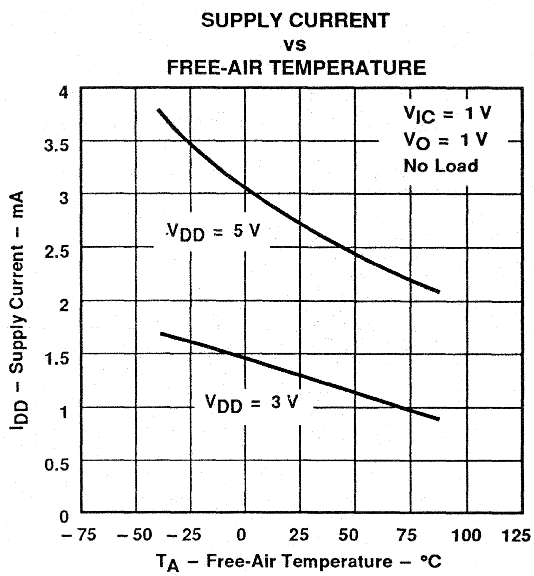


Figure 18

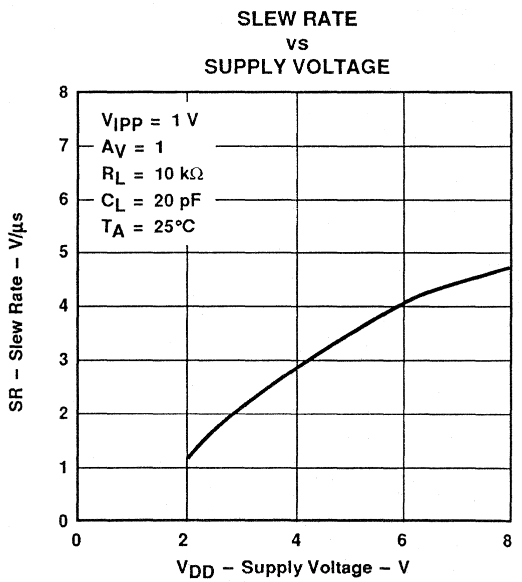


Figure 19

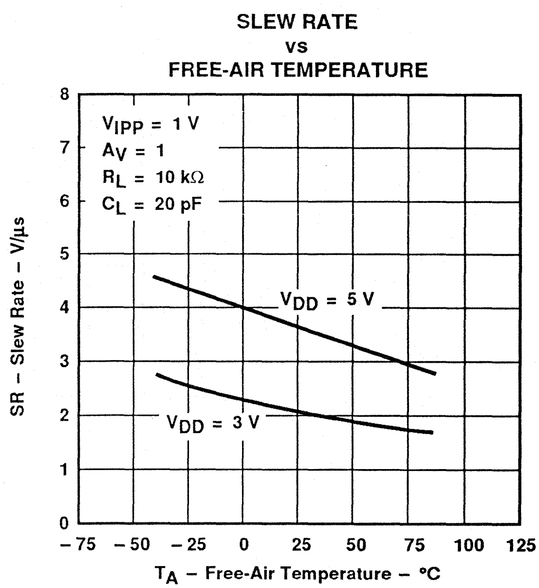


Figure 20

TYPICAL CHARACTERISTICS

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

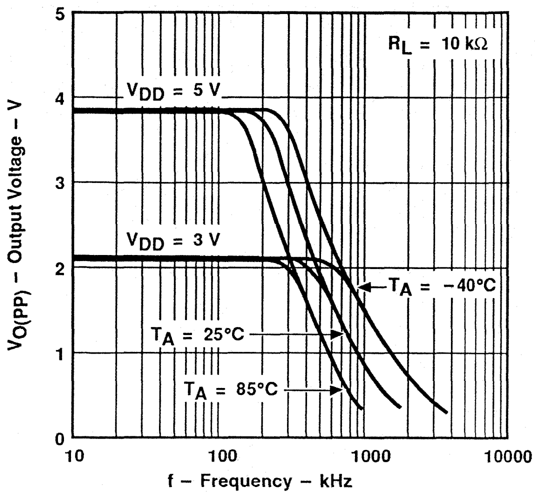


Figure 21

UNITY-GAIN BANDWIDTH
vs
FREE-AIR TEMPERATURE

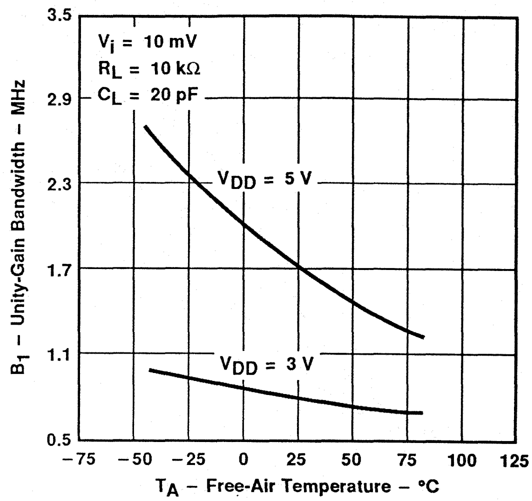


Figure 22

UNITY-GAIN BANDWIDTH
vs
SUPPLY VOLTAGE

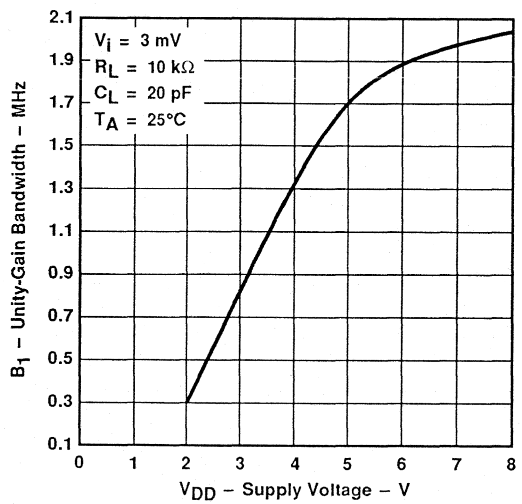


Figure 23

TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

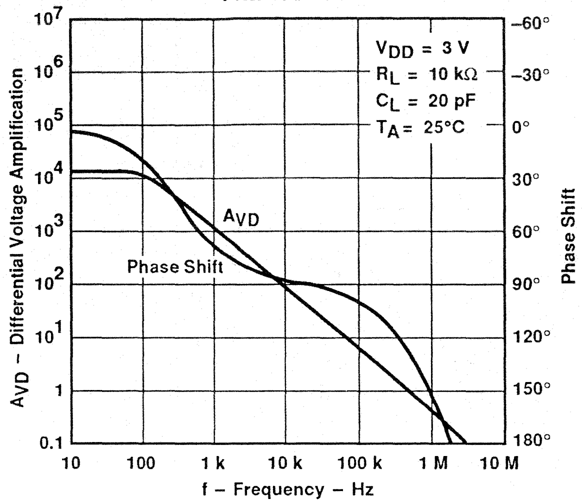


Figure 24

LARGE-SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT
vs
FREQUENCY

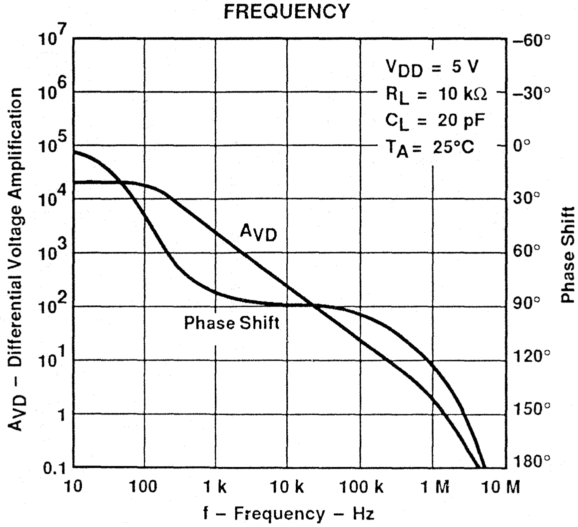


Figure 25

TYPICAL CHARACTERISTICS

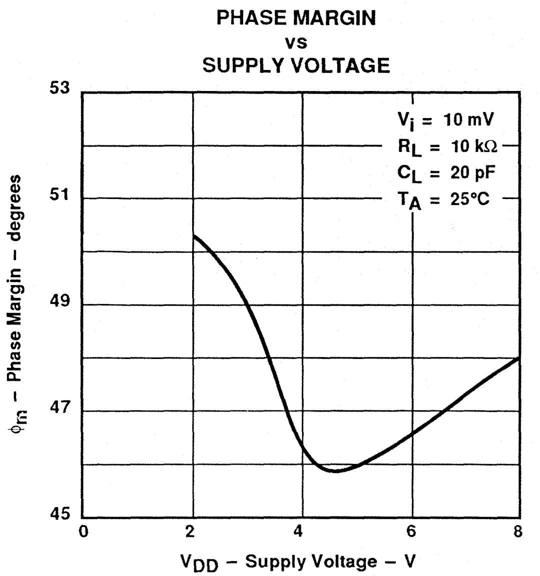


Figure 26

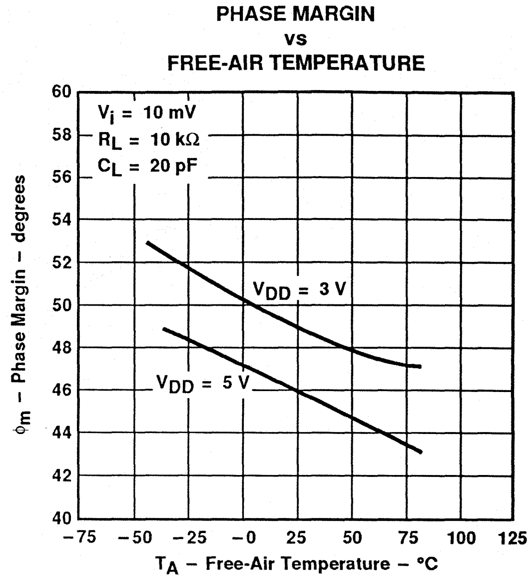


Figure 27

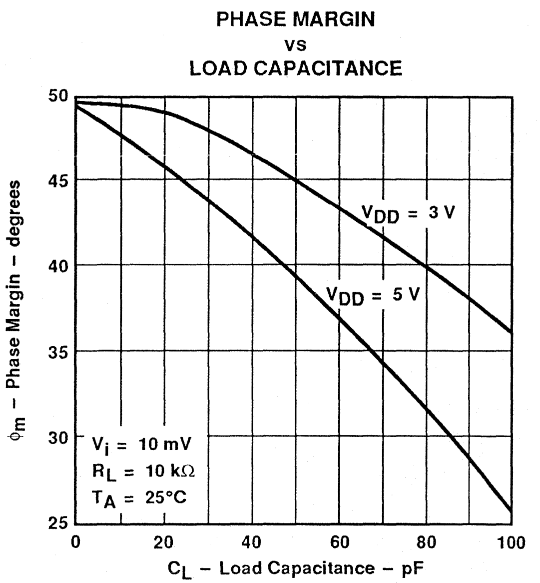


Figure 28

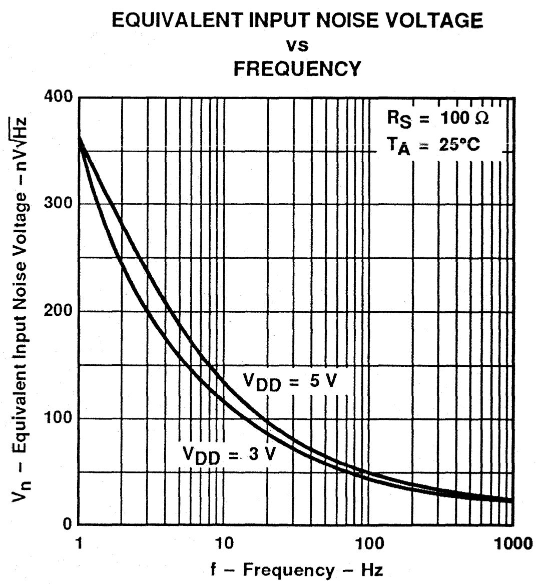
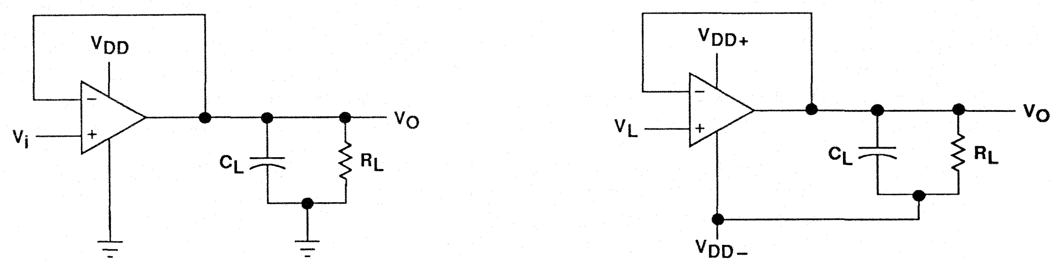


Figure 29

PARAMETER MEASUREMENT INFORMATION

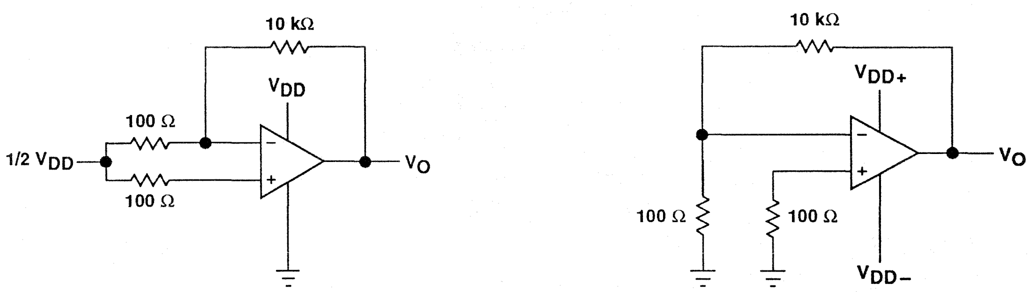
single-supply versus split-supply test circuits

Because the TLV2344 is optimized for single-supply operation, circuit configurations used for the various tests often present some inconvenience since the input signal, in many cases, must be offset from ground. This inconvenience can be avoided by testing the device with split supplies and the output load tied to the negative rail. A comparison of single-supply versus split-supply test circuits is shown below. The use of either circuit will give the same result.



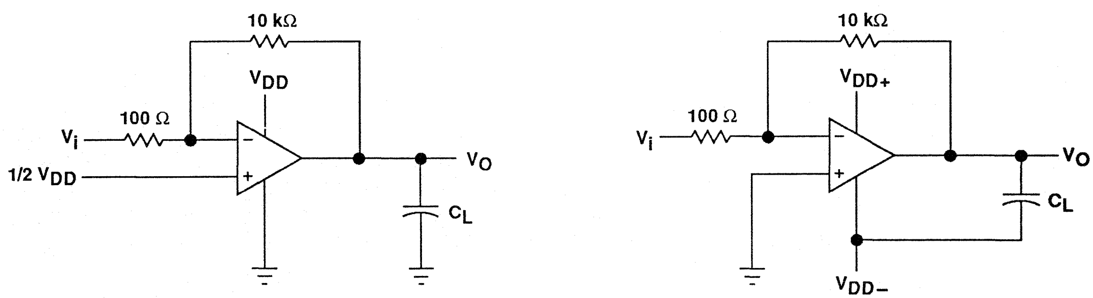
(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 30. Unity-Gain Amplifier



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 31. Noise Test Circuit



(a) SINGLE-SUPPLY (b) SPLIT-SUPPLY

Figure 32. Gain-of-100 Inverting Amplifier

PARAMETER MEASUREMENT INFORMATION

input bias current

Because of the high input impedance of the TLV2344 operational amplifier, attempts to measure the input bias current can result in erroneous readings. The bias current at normal ambient temperature is typically less than 1 pA, a value that is easily exceeded by leakages on the test socket. Two suggestions are offered to avoid erroneous measurements:

1. Isolate the device from other potential leakage sources. Use a grounded shield around and between the device inputs (see Figure 33). Leakages that would otherwise flow to the inputs will be shunted away.

2. Compensate for the leakage of the test socket by actually performing an input bias current test (using a picoammeter) with no device in the test socket. The actual input bias current can then be calculated by subtracting the open-socket leakage readings from the readings obtained with a device in the test socket.

   One word of caution, many automatic testers as well as some bench-top operational amplifier testers use the servo-loop technique with a resistor in series with the device input to measure the input bias current (the voltage drop across the series resistor is measured and the bias current is calculated). This method requires that a device be inserted into the test socket to obtain a correct reading; therefore, an open-socket reading is not feasible using this method.

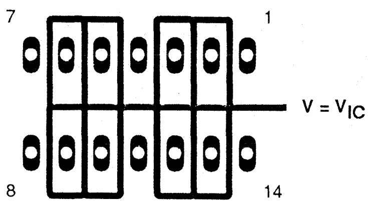


Figure 33. Isolation Metal Around Device Inputs (N Dual-In-Line Package)

low-level output voltage

To obtain low-supply-voltage operation, some compromise is necessary in the input stage. This compromise results in the device low-level output being dependent on both the common-mode input voltage level as well as the differential input voltage level. When attempting to correlate low-level output readings with those quoted in the electrical specifications, these two conditions should be observed. If conditions other than these are to be used, please refer to the Typical Characteristics section of this data sheet.

input offset voltage temperature coefficient

Erroneous readings often result from attempts to measure temperature coefficient of input offset voltage. This parameter is actually a calculation using input offset voltage measurements obtained at two different temperatures. When one (or both) of the temperatures is below freezing, moisture can collect on both the device and the test socket. This moisture will result in leakage and contact resistance which can cause erroneous input offset voltage readings. The isolation techniques previously mentioned have no effect on the leakage since the moisture also covers the isolation metal itself, thereby rendering it useless. It is suggested that these measurements be performed at temperatures above freezing to minimize error.

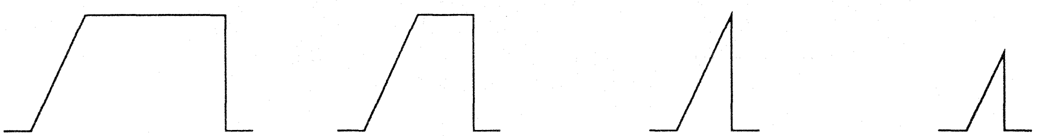
full power response

Full power response, the frequency above which the operational amplifier slew rate limits the output voltage swing, is often specified two ways: full-linear response and full-peak response. The full-linear response is

PARAMETER MEASUREMENT INFORMATION

generally measured by monitoring the distortion level of the output while increasing the frequency of a sinusoidal input signal until the maximum frequency is found above which the output contains significant distortion. The full-peak response is defined as the maximum output frequency, without regard to distortion, above which full peak-to-peak output swing cannot be maintained.

Because there is no industry-wide accepted value for significant distortion, the full-peak response is specified in this data sheet and is measured using the circuit of Figure 30. The initial setup involves the use of a sinusoidal input to determine the maximum peak-to-peak output of the device (the amplitude of the sinusoidal wave is increased until clipping occurs). The sinusoidal wave is then replaced with a square wave of the same amplitude. The frequency is then increased until the maximum peak-to-peak output can no longer be maintained (Figure 34). A square wave is used to allow a more accurate determination of the point at which the maximum peak-to-peak output is reached.



(a) f = 100 Hz (b) B_{OM} > f > 100 Hz (c) f = B_{OM} (d) f > B_{OM}

Figure 34. Full-Power-Response Output Signal

test time

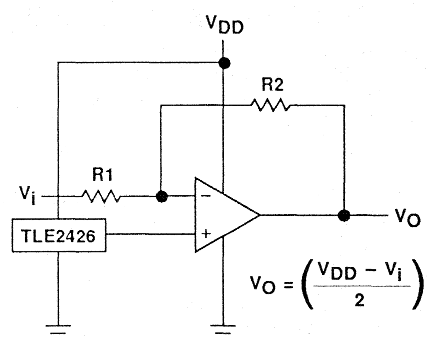
Inadequate test time is a frequent problem, especially when testing CMOS devices in a high-volume, short-test-time environment. Internal capacitances are inherently higher in CMOS than in bipolar and BiFET devices, and require longer test times than their bipolar and BiFET counterparts. The problem becomes more pronounced with reduced supply levels and lower temperatures.

TYPICAL APPLICATION DATA

single-supply operation

While the TLV2344 will perform well using dual-power supplies (also called balanced or split supplies), the design is optimized for single-supply operation. This includes an input common-mode voltage range that encompasses ground as well as an output voltage range that pulls down to ground. The supply voltage range extends down to 2 V, thus allowing operation with supply levels commonly available for TTL and HCMOS.

Many single-supply applications require that a voltage be applied to one input to establish a reference level that is above ground. This virtual ground can be generated using two large resistors, but a prefered technique is to use a virtual ground generator such as the TLE2426. The TLE2426 supplies an accurate voltage equal to $V_{DD}/2$, while consuming very little power, and is suitable for supply voltages of greater than 4 V.



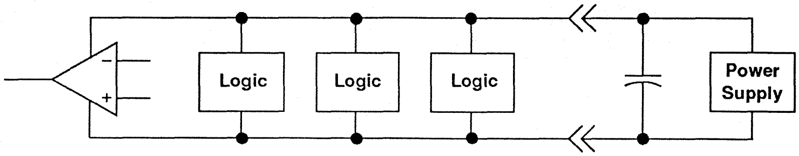
$$V_O = \left(\frac{V_{DD} - V_i}{2}\right)\frac{R_2}{R_1} + \frac{V_{DD}}{2}$$

Figure 35. Inverting Amplifier With Voltage Reference

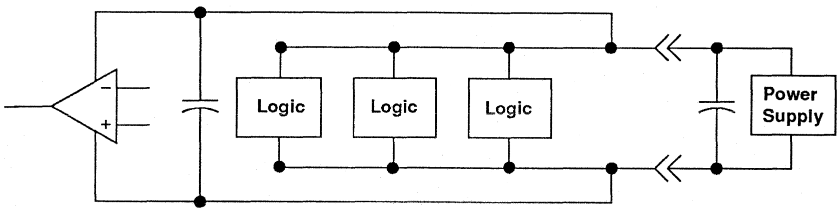
TYPICAL APPLICATION DATA

The TLV2344 works well in conjunction with digital logic; however, when powering both linear devices and digital logic from the same power supply, the following precautions are recommended:

1. Power the linear devices from separate bypassed supply lines (see Figure 36); otherwise, the linear device supply rails can fluctuate due to voltage drops caused by high switching currents in the digital logic.
2. Use proper bypass techniques to reduce the probability of noise-induced errors. Single capacitive decoupling is often adequate; however, RC decoupling may be necessary in high-frequency applications.



(a) COMMON SUPPLY RAILS



(b) SEPARATE BYPASSED SUPPLY RAILS (PREFERRED)

Figure 36. Common Versus Separate Supply Rails

input characteristics

The TLV2344 is specified with a minimum and a maximum input voltage that, if exceeded at either input, could cause the device to malfunction. Exceeding this specified range is a common problem, especially in single-supply operation. Note that the lower range limit includes the negative rail, while the upper range limit is specified at $V_{DD} - 1$ V at $T_A = 25°C$ and at $V_{DD} - 1.2$ V at all other temperatures.

The use of the polysilicon-gate process and the careful input circuit design gives the TLV2344 very good input offset voltage drift characteristics relative to conventional metal-gate processes. Offset voltage drift in CMOS devices is highly influenced by threshold voltage shifts caused by polarization of the phosphorus dopant implanted in the oxide. Placing the phosphorus dopant in a conductor (such as a polysilicon gate) alleviates the polarization problem, thus reducing threshold voltage shifts by more than an order of magnitude. The offset voltage drift with time has been calculated to be typically 0.1 μV/month, including the first month of operation.

Because of the extremely high input impedance and resulting low-bias current requirements, the TLV2344 is well suited for low-level signal processing; however, leakage currents on printed circuit boards and sockets can easily exceed bias-current requirements and cause a degradation in device performance. It is good practice to include guard rings around inputs (similar to those of Figure 33 in the Parameter Measurment Information section). These guards should be driven from a low-impedance source at the same voltage level as the common-mode input (see Figure 37).

The inputs of any unused amplifiers should be tied to ground to avoid possible oscillation.

TYPICAL APPLICATION DATA

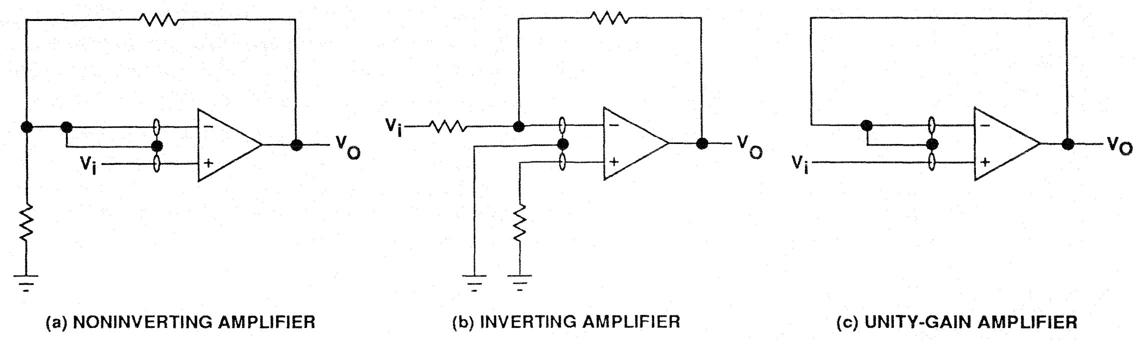


Figure 37. Guard Ring Schemes

noise performance

The noise specifications in operational amplifier circuits are greatly dependent on the current in the first-stage differential amplifier. The low input bias current requirements of the TLV2344 results in a very low noise current, which is insignificant in most applications. This feature makes the devices especially favorable over bipolar devices when using values of circuit impedance greater than 50 kΩ, since bipolar devices exhibit greater noise currents.

feedback

Operational amplifier circuits nearly always employ feedback, and since feedback is the first prerequisite for oscillation, a little caution is appropriate. Most oscillation problems result from driving capacitive loads and ignoring stray input capacitance. A small-value capacitor connected in parallel with the feedback resistor is an effective remedy (see Figure 38). The value of this capacitor is optimized empirically.

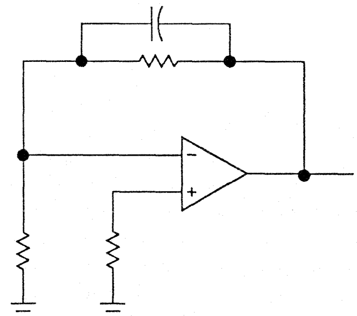


Figure 38. Compensation for Input Capacitance

electrostatic discharge protection

The TLV2344 incorporates an internal electrostatic discharge (ESD) protection circuit that will prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2. Care should be exercised, however, when handling these devices as exposure to ESD may result in the degradation of the device parametric performance. The protection circuit also causes the input bias currents to be temperature dependent and have the characteristics of a reverse-biased diode.

latch-up

Because CMOS devices are susceptible to latch-up due to their inherent parasitic thyristors, the TLV2344 inputs and output are designed to withstand −100-mA surge currents without sustaining latch-up; however, techniques should be used to reduce the chance of latch-up whenever possible. Internal protection diodes

TYPICAL APPLICATION DATA

should not by design be forward biased. Applied input and output voltage should not exceed the supply voltage by more than 300 mV. Care should be exercised when using capacitive coupling on pulse generators. Supply transients should be shunted by the use of decoupling capacitors (0.1 µF typical) located across the supply rails as close to the device as possible.

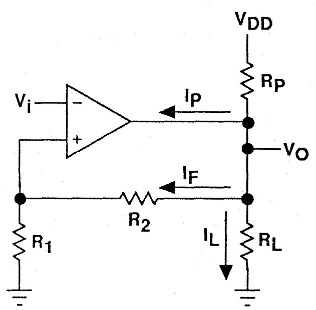
The current path established if latch-up occurs is usually between the positive supply rail and ground and can be triggered by surges on the supply lines and/or voltages on either the output or inputs that exceed the supply voltage. Once latch-up occurs, the current flow is limited only by the impedance of the power supply and the forward resistance of the parasitic thyristor and usually results in the destruction of the device. The chance of latch-up occuring increases with increasing temperature and supply voltages.

output characteristics

The output stage of the TLV2344 is designed to sink and source relatively high amounts of current (see Typical Characteristics). If the output is subjected to a short-circuit condition, this high-current capability can cause device damage under certain conditions. Output current capability increases with supply voltage.

Although theTLV2344 possesses excellent high-level output voltage and current capability, methods are available for boosting this capability, if needed. The simplest method involves the use of a pullup resistor (R_P) connected from the output to the positive supply rail (see Figure 39). There are two disadvantages to the use of this circuit. First, the NMOS pulldown transistor, N4 (see equivalent schematic) must sink a comparatively large amount of current. In this circuit, N4 behaves like a linear resistor with an on-resistance between approximately 60 Ω and 180 Ω, depending on how hard the operational amplifier input is driven. With very low values of R_P, a voltage offset from 0 V at the output will occur. Secondly, pullup resistor R_P acts as a drain load to N4 and the gain of the operational amplifier is reduced at output voltage levels where N5 is not supplying the output current.

All operating characteristics of the TLV2344 are measured using a 20-pF load. The devices will drive higher capacitive loads; however, as output load capacitance increases, the resulting response pole occurs at lower frequencies, thereby causing ringing, peaking, or even oscillation (see Figures 41, 42, and 43). In many cases, adding some compensation in the form of a series resistor in the feedback loop will alleviate the problem.



$$R_P = \frac{V_{DD} - V_O}{I_F + I_L + I_P}$$

I_P = Pullup current required by the operational amplifier (typically 500 µA)

Figure 39. Resistive Pullup to Increase V_{OH}

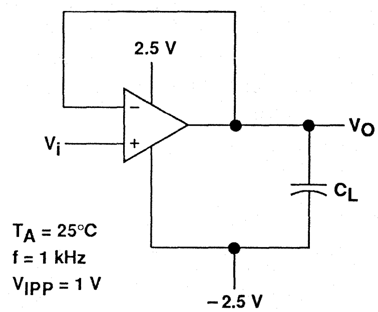
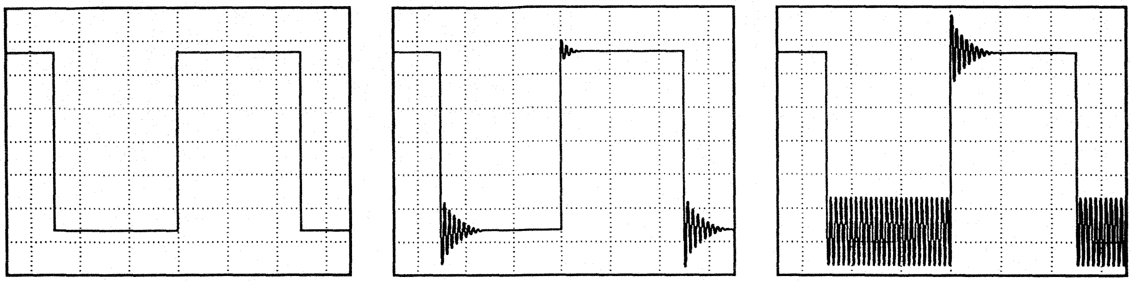


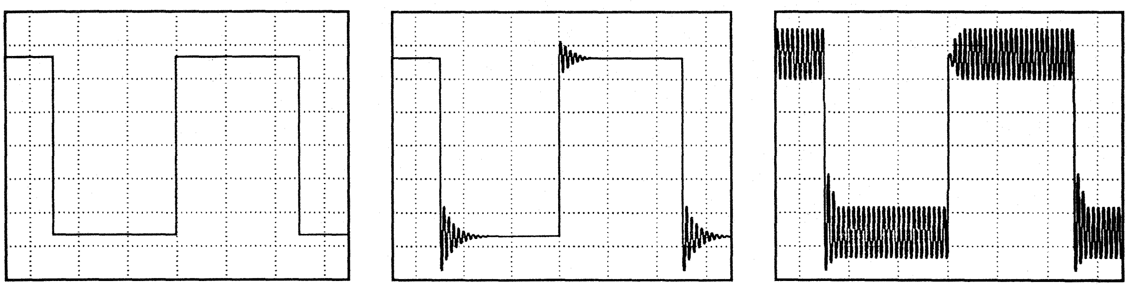
Figure 40. Test Circuit for Output Characteristics

TYPICAL APPLICATION DATA



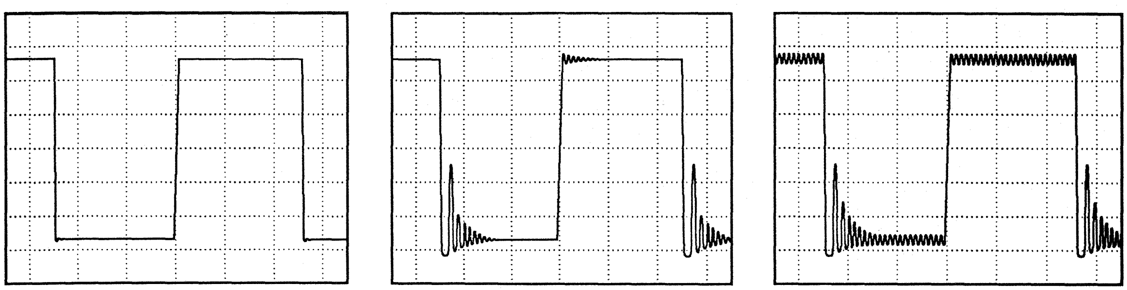
(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 130 pF, R_L = NO LOAD (c) C_L = 150 pF, R_L = NO LOAD

Figure 41. Effect of Capacitive Loads in High-Bias Mode



(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 170 pF, R_L = NO LOAD (c) C_L = 190 pF, R_L = NO LOAD

Figure 42. Effect of Capacitive Loads in Medium-Bias Mode

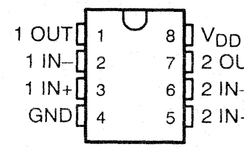


(a) C_L = 20 pF, R_L = NO LOAD (b) C_L = 260 pF, R_L = NO LOAD (c) C_L = 310 pF, R_L = NO LOAD

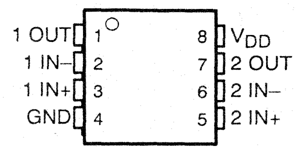
Figure 43. Effect of Capacitive Loads in Low-Bias Mode

- Wide Range of Supply Voltages
  2 V to 8 V
- Fully Characterized at 3 V and 5 V
- Very Low Supply Current Drain
  120 μA Typ at 3 V
- Output Compatible With TTL, MOS, and CMOS
- Fast Response Time . . . 200 ns Typ for TTL-Level Input Step
- High Input Impedance . . . 10^{12} Ω Typ
- Extremely Low Input Bias Current
  5 pA Typ
- Common-Mode Input Voltage Range Includes Ground
- Built-In ESD Protection

D OR P PACKAGE
(TOP VIEW)

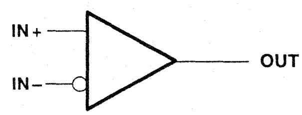


PW PACKAGE
(TOP VIEW)



NC — No internal connection

symbol (each comparator)



description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power supply applications and to operate with power supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μA.

The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352 is fully characterized at 3 V and 5 V for operation from – 40°C to 85°C.

The TLV2352 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)†	PLASTIC DIP (P)	TSSOP (PW)‡	
–40°C to 85°C	5 mV	TLV2352ID	TLV2352IP	TLV2352IPW	TLV2352Y

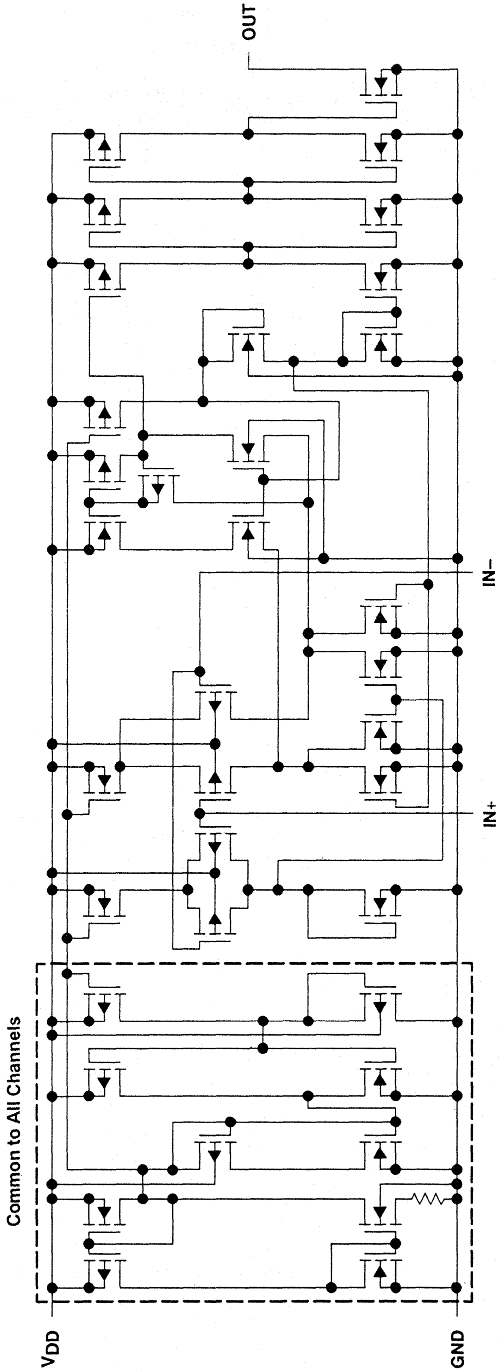
† The D package is available taped and reeled. Add the suffix "R" to the device type (e.g., TLV2352IDR).
‡ PW packages are only available left-ended taped and reeled, (e.g., TLV2352IPWLE)

This device has limited built-in gate protection. The leads should be shorted together or the device should be placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

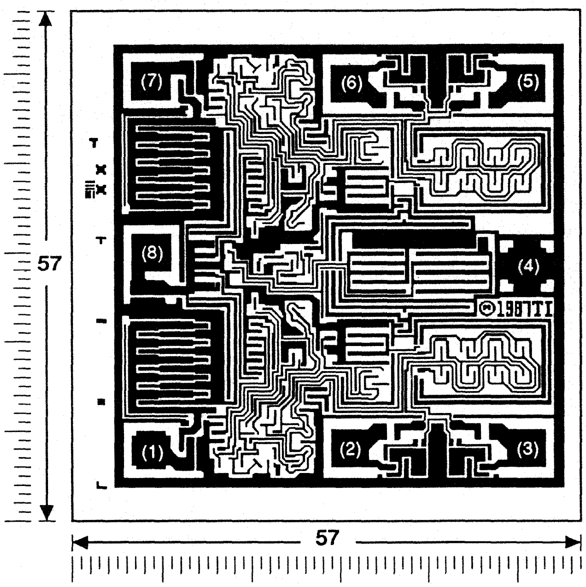
equivalent schematic

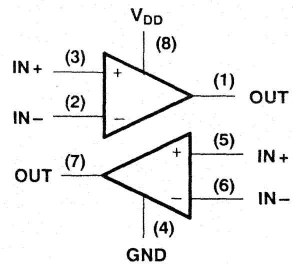


TLV2352Y chip information

These chips, properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	± 8 V
Input voltage range, V_I	− 0.3 to 8 V
Output voltage, V_O	8 V
Input current, I_I	± 5 mA
Output current, I_O	20 mA
Duration of output short circuit to ground (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	− 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package	260°C

† Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		I-SUFFIX MIN	I-SUFFIX MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	V
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS	T_A‡	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 4	25°C		1	5		1	5	mV
			Full range			7			7	
I_{IO}	Input offset current		25°C		1			1		pA
			85°C			1			1	nA
I_{IB}	Input bias current		25°C		5			5		pA
			85°C			2			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to 2			0 to 4			V
			Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V	25°C		0.1			0.1		nA
			Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 2 mA	25°C		115	300		150	400	mV
			Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V, No load	25°C		120	250		140	300	µA
			Full range			350			400	

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

§ C_L includes probe and jig capacitance.

NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		V_{DD} = 3 V MIN	TYP	MAX	V_{DD} = 5 V MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4			1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 2 mA		115	300		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V	No load		120	250		140	300	μA

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

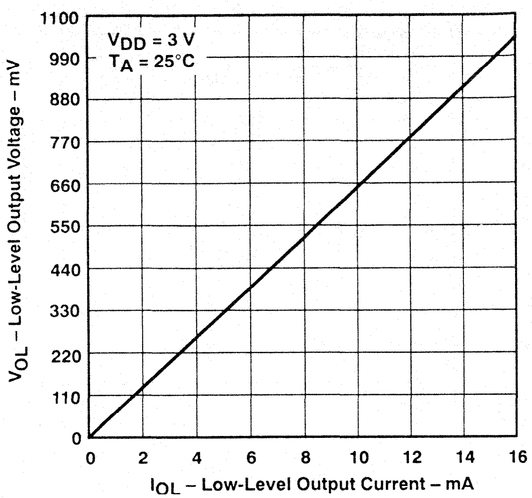


Figure 1

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

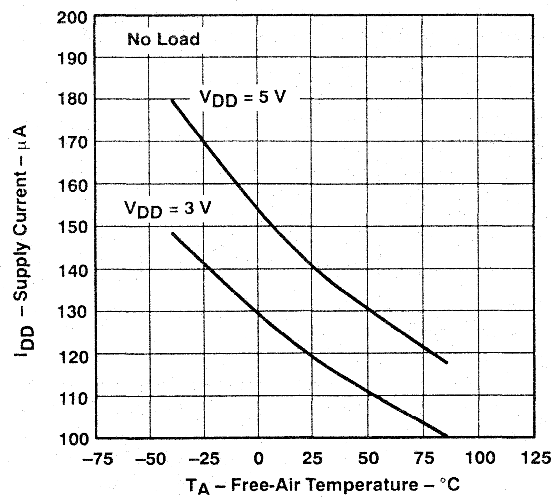


Figure 2

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

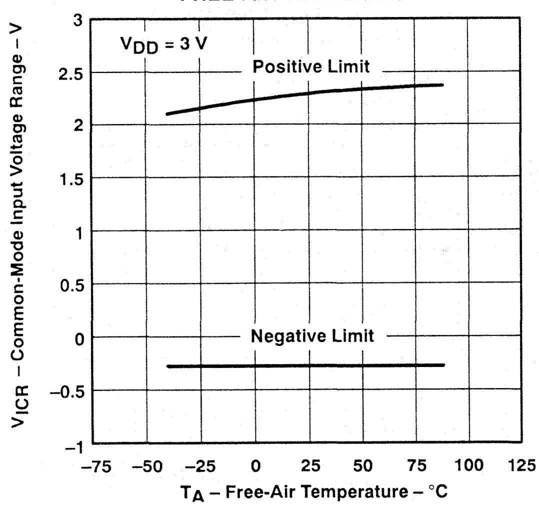


Figure 3

OUTPUT FALL TIME
vs
CAPACITIVE LOAD

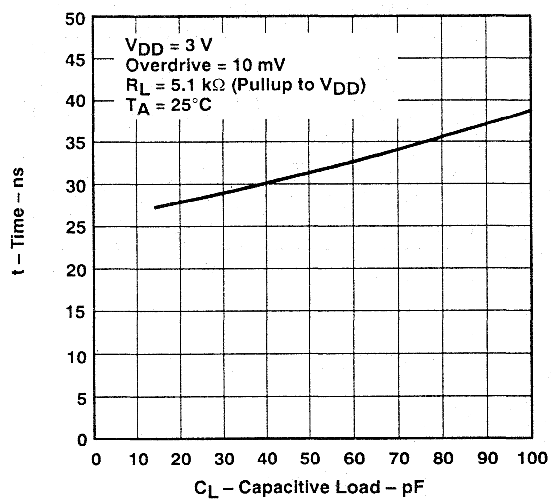


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

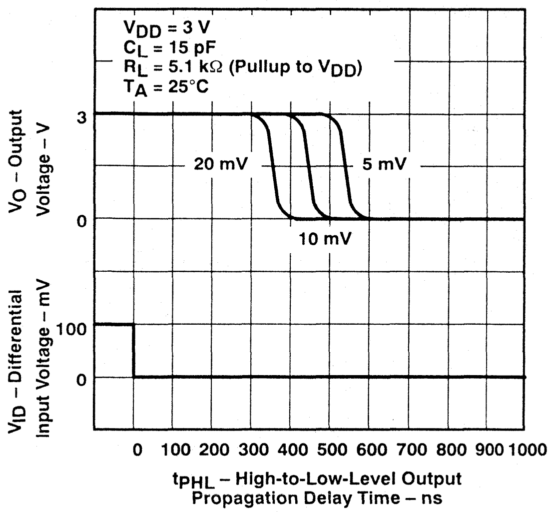


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

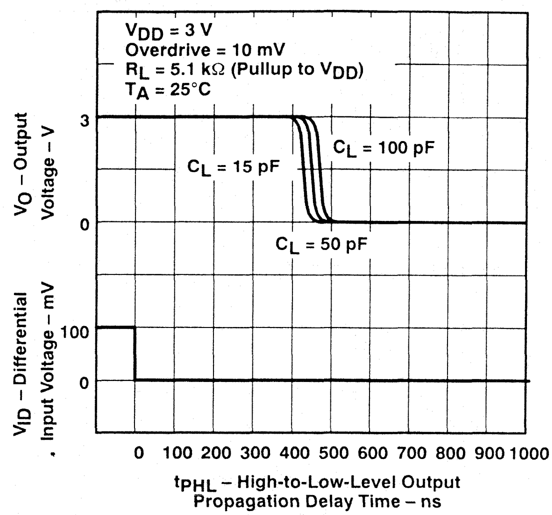


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

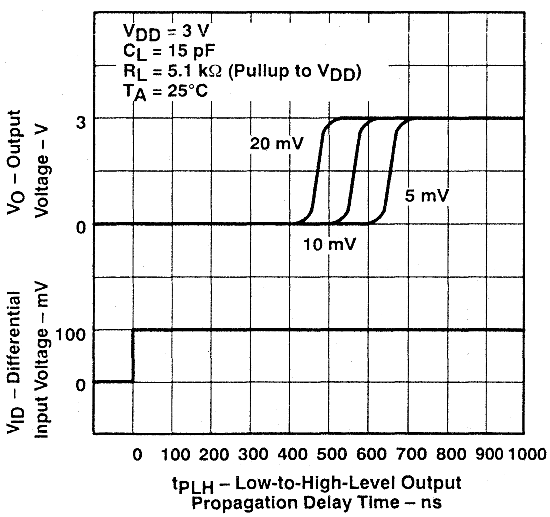


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

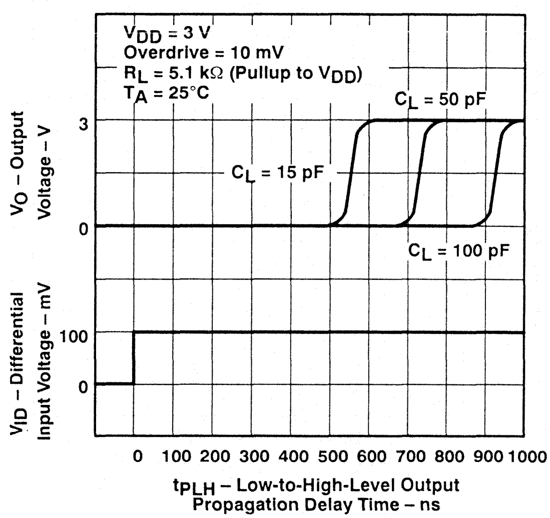


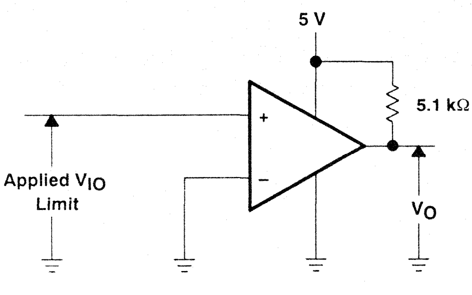
Figure 8

PARAMETER MEASUREMENT INFORMATION

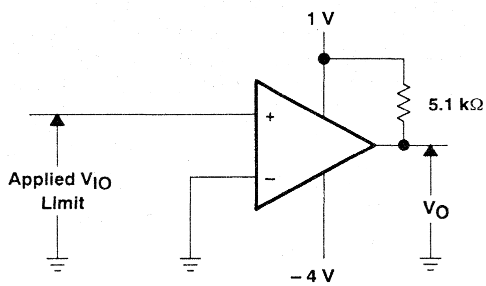
The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.



(a) V_{IO} WITH $V_{IC} = 0$



(b) V_{IO} WITH V_{IC} = 4 V

Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

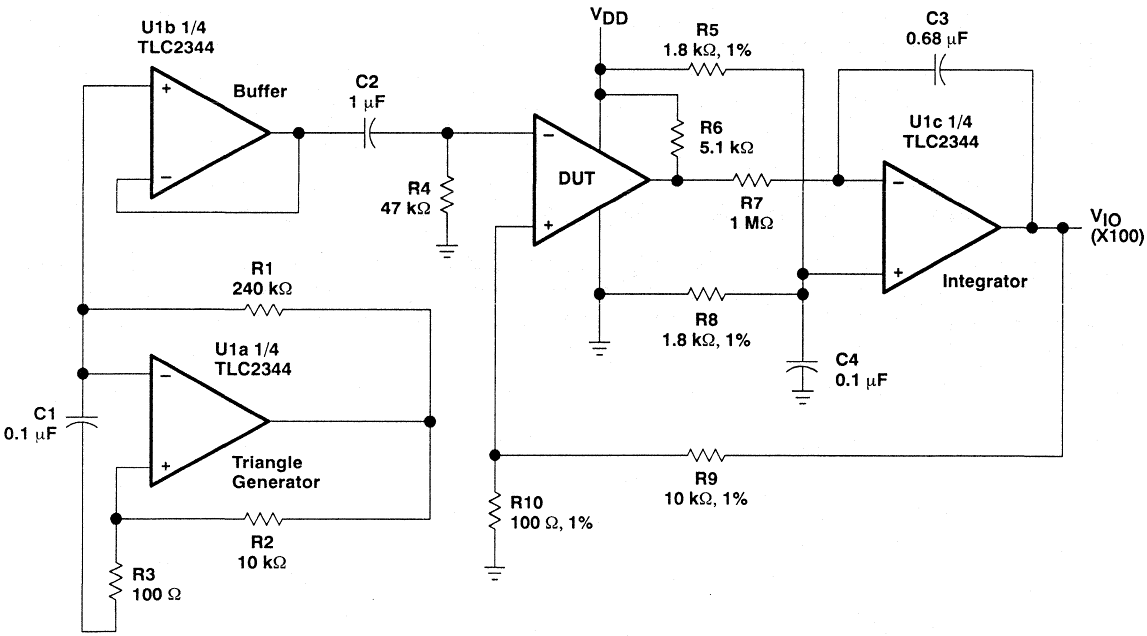
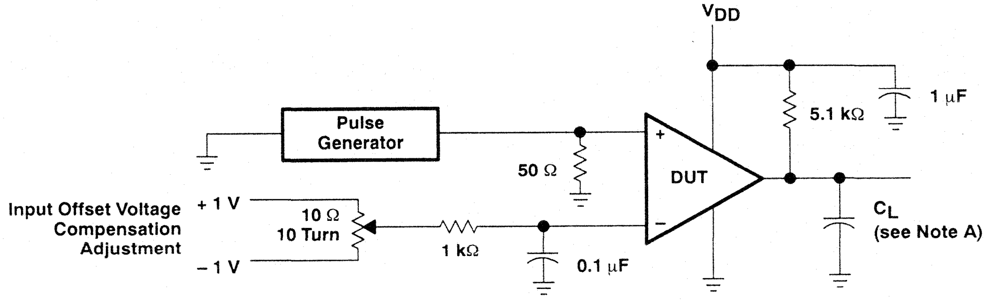


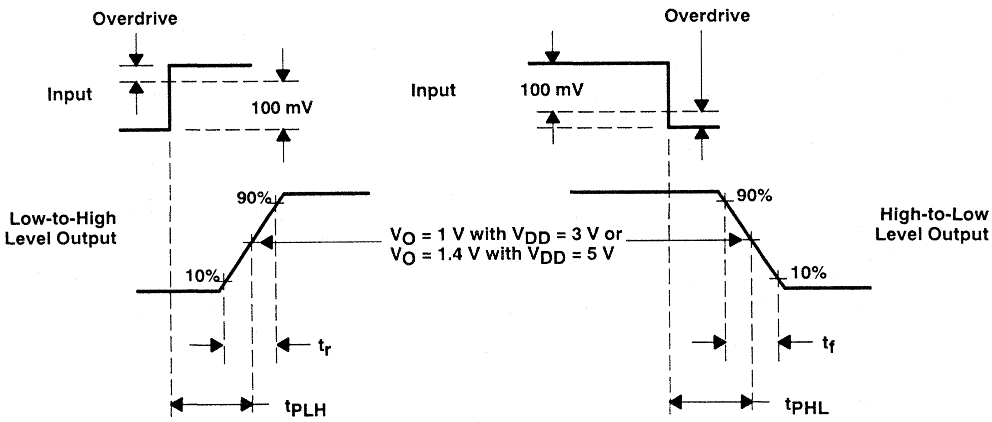
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

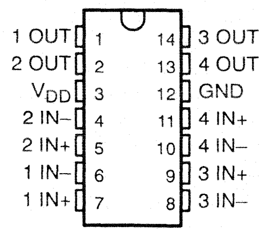
Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

TLV2354I, TLV2354Y
LinCMOS™ QUADRUPLE LOW-VOLTAGE DIFFERENTIAL COMPARATORS

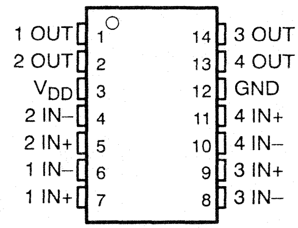
SLCS012–D4017, MAY 1992

- **Wide Range of Supply Voltages**
  2 V to 8 V
- **Fully Characterized at 3 V and 5 V**
- **Very Low Supply Current Drain**
  240 μA Typ at 3 V
- **Common-Mode Input Voltage Range Includes Ground**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current**
  5 pA Typ
- **Output Compatible With TTL, MOS, and CMOS**
- **Built-In ESD Protection**

D OR N PACKAGE
(TOP VIEW)



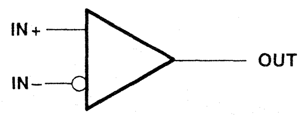
PW PACKAGE
(TOP VIEW)



description

The TLV2354 consists of four independent, low-power comparators specifically designed for single power supply applications and to operate with power supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 240 μA.

symbol (each comparator)



The TLV2354 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2354 is fully characterized for operation from – 40°C to 85°C.

The TLV2354 has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

T_A	V_{IO} max at 25°C	PACKAGE			CHIP FORM (Y)
		SMALL OUTLINE (D)†	PLASTIC DIP (N)	TSSOP (PW)‡	
–40°C to 85°C	5 mV	TLV2354ID	TLV2354IN	TLV2354IPW	TLV2354Y

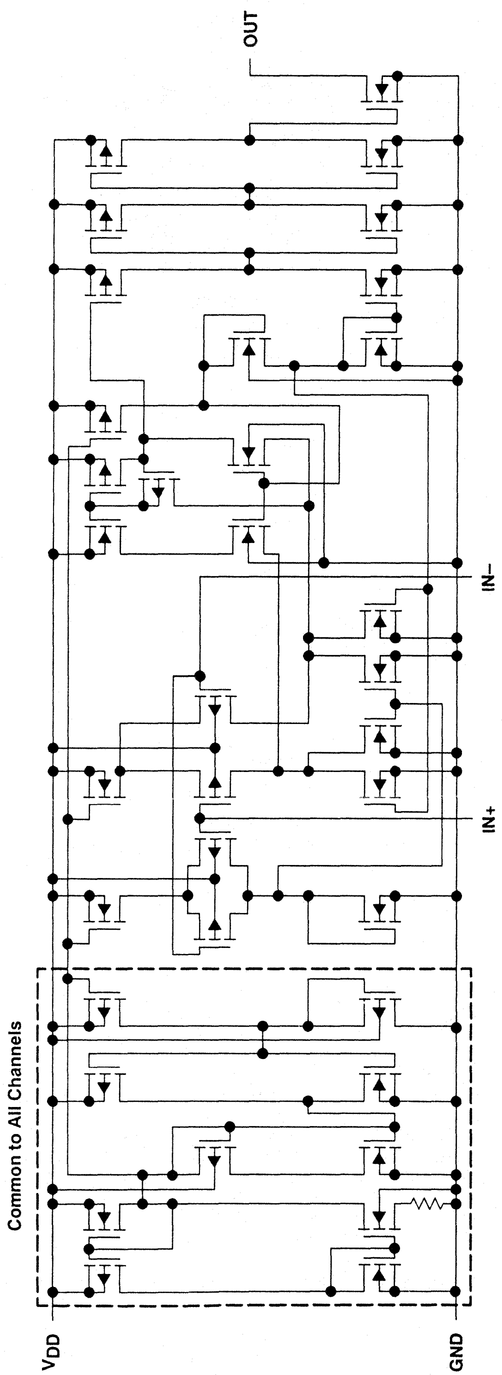
† The D package is available taped and reeled. Add the suffix “R” to the device type (e.g., TLV2352IDR).
‡ PW packages are only available left-ended taped and reeled, (e.g., TLV2354IPWLE)

This device has limited built-in gate protection. During storage or handling, the device leads should be shorted together or the device should be placed in conductive foam.

LinCMOS is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

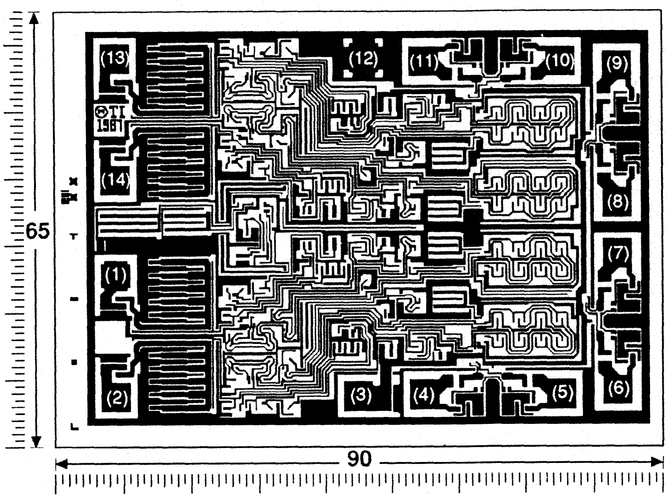
equivalent schematic

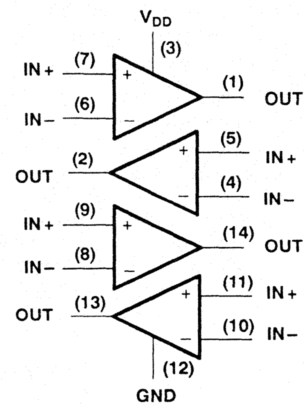


TLV2354Y chip information

These chips, properly assembled, display characteristics similar to the TLV2354. Thermal compression or ultrasonic bonding may be used on the doped aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

T_{JMAX} = 150°C

TOLERANCES ARE ±10%

ALL DIMENSIONS ARE IN MILS

PIN (11) INTERNALLY CONNECTED TO BACKSIDE OF CHIP

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1)	8 V
Differential input voltage, V_{ID} (see Note 2)	± 8 V
Input voltage range, V_I	– 0.3 to 8 V
Output voltage, V_O	8 V
Input current, I_I	± 5 mA
Output current, I_O	20 mA
Duration of output short circuit to ground (see Note 3)	unlimited
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range	–40°C to 85°C
Storage temperature range	– 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, N, or PW package	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at the noninverting input terminal with respect to the inverting input terminal.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	950 mW	7.6 mW/°C	494 mW
N	1150 mW	9.2 mW/°C	598 mW
PW	700 mW	5.6 mW/°C	346 mW

recommended operating conditions

		I-SUFFIX		UNIT
		MIN	MAX	
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	
Operating free-air temperature, T_A		–40	85	°C

electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS	T_A‡	V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$ min, See Note 4	25°C		1	5		1	5	mV
			Full range			7			7	
I_{IO}	Input offset current		25°C		1			1		pA
			85°C			1			1	nA
I_{IB}	Input bias current		25°C		5			5		pA
			85°C			2			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to 2			0 to 4			V
			Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V	25°C		0.1			0.1		nA
			Full range			1			1	μA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 2 mA	25°C		115	300		150	400	mV
			Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V, No load	25°C		240	500		290	600	μA
			Full range			700			800	

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Response time	R_L = 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

§ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		V_{DD} = 3 V			V_{DD} = 5 V			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4			1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 2 mA		115	300		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V	No load		240	500		290	600	μA

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

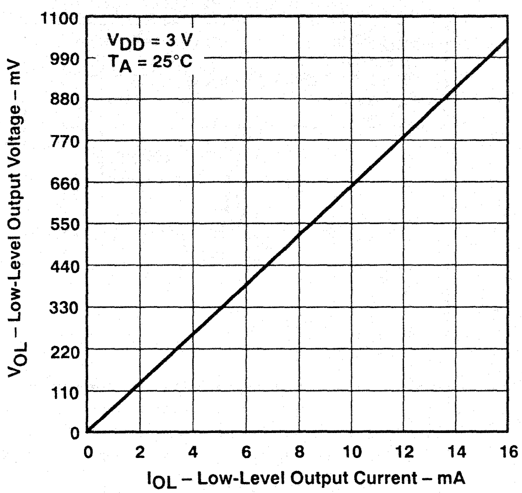


Figure 1

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

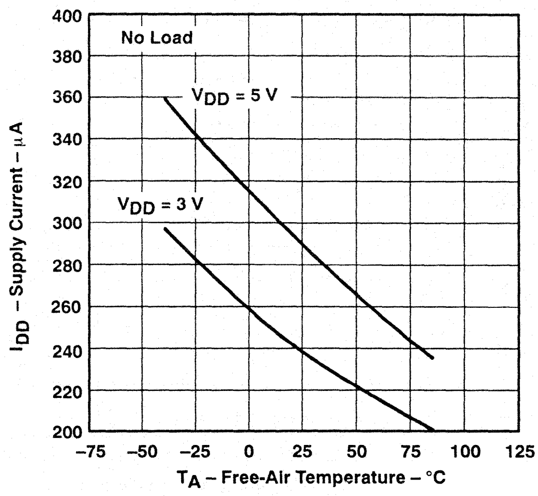


Figure 2

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

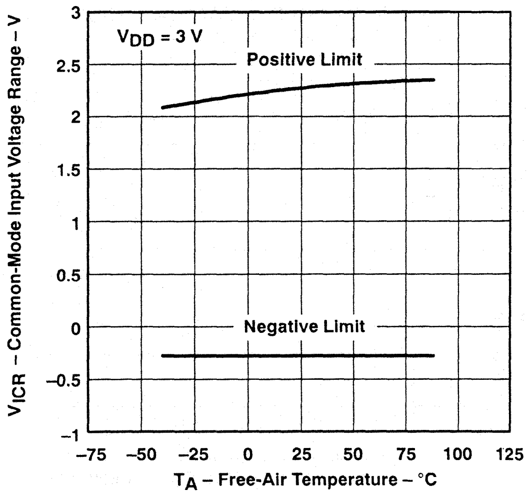


Figure 3

OUTPUT FALL TIME
vs
CAPACITIVE LOAD

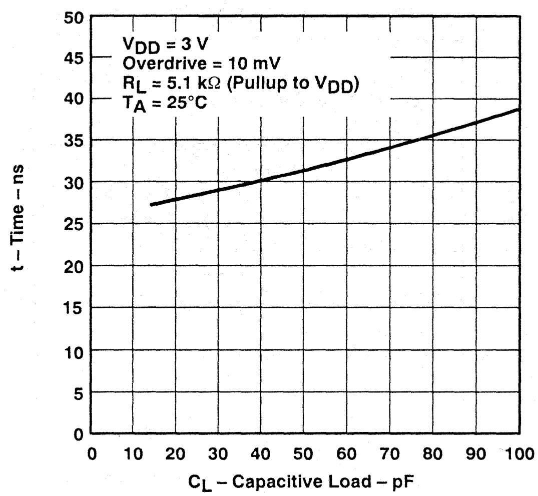


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

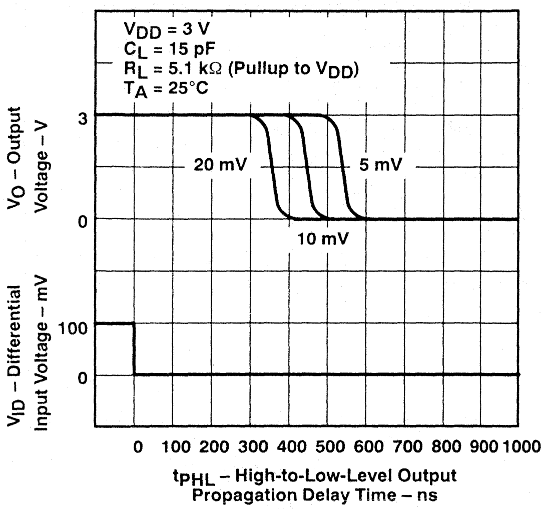


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS CAPACITIVE LOADS

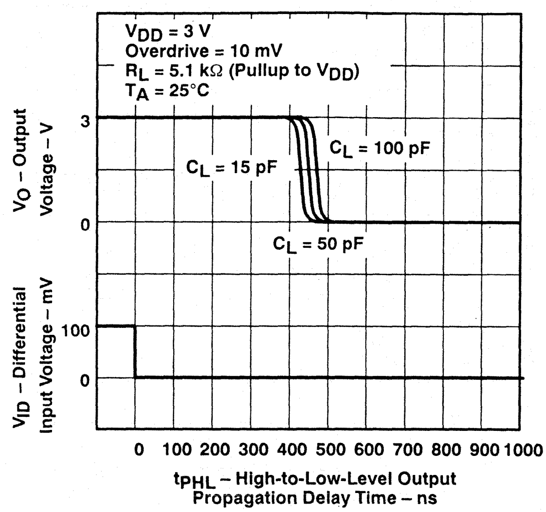


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS OVERDRIVE VOLTAGES

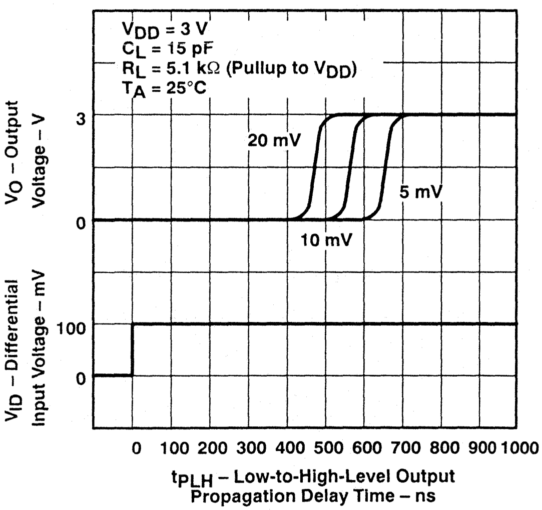


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT PROPAGATION DELAY FOR VARIOUS CAPACITIVE LOADS

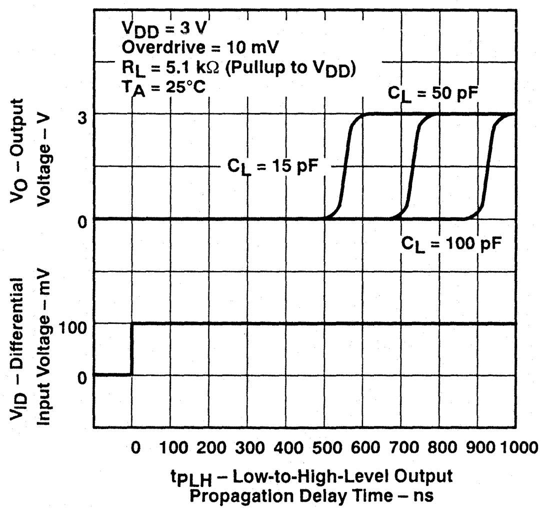


Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2354 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure1 (a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure1 (b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.

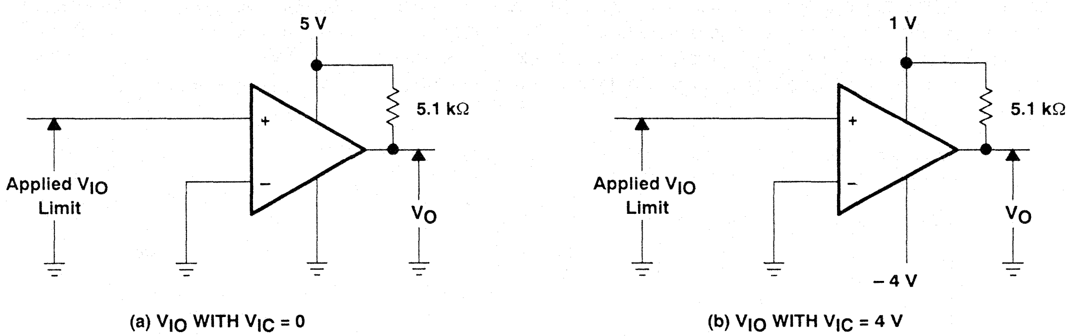


Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output will change states.

PARAMETER MEASUREMENT INFORMATION

Figure 2 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer, with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage divider R9 and R10 provides a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

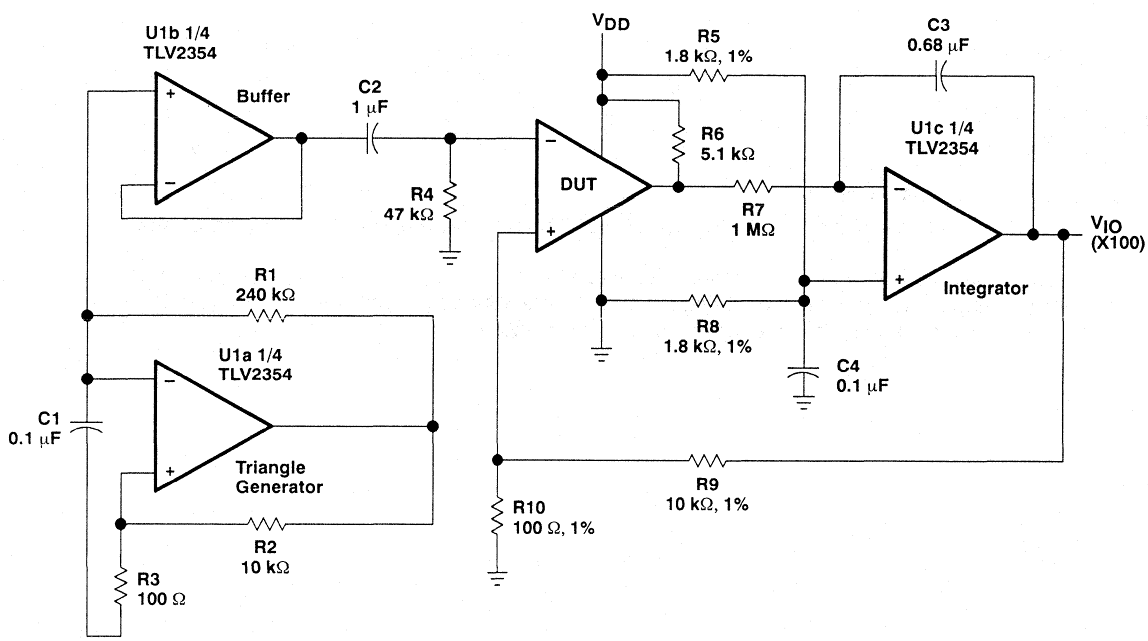
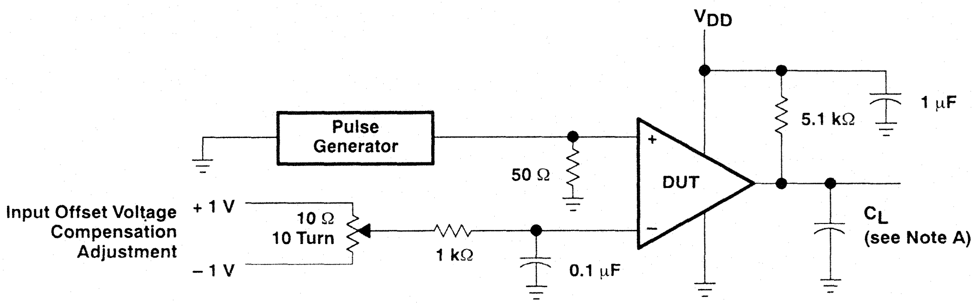


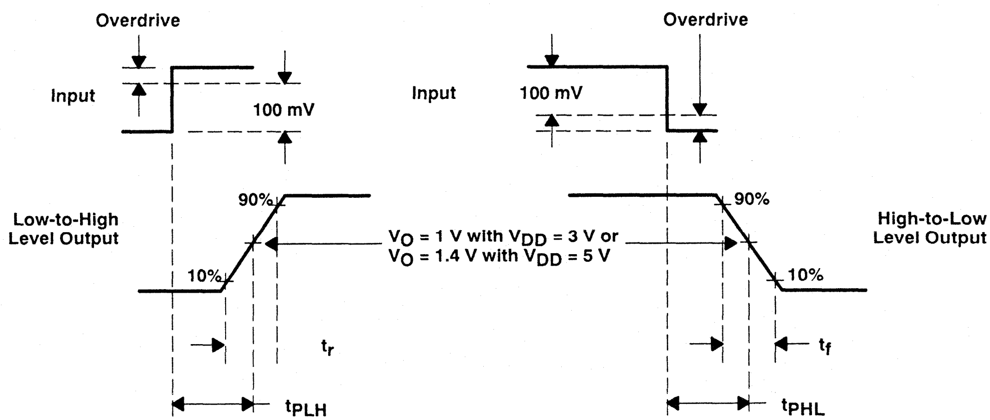
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse, while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation delay time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 3) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, will cause the output to change state.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

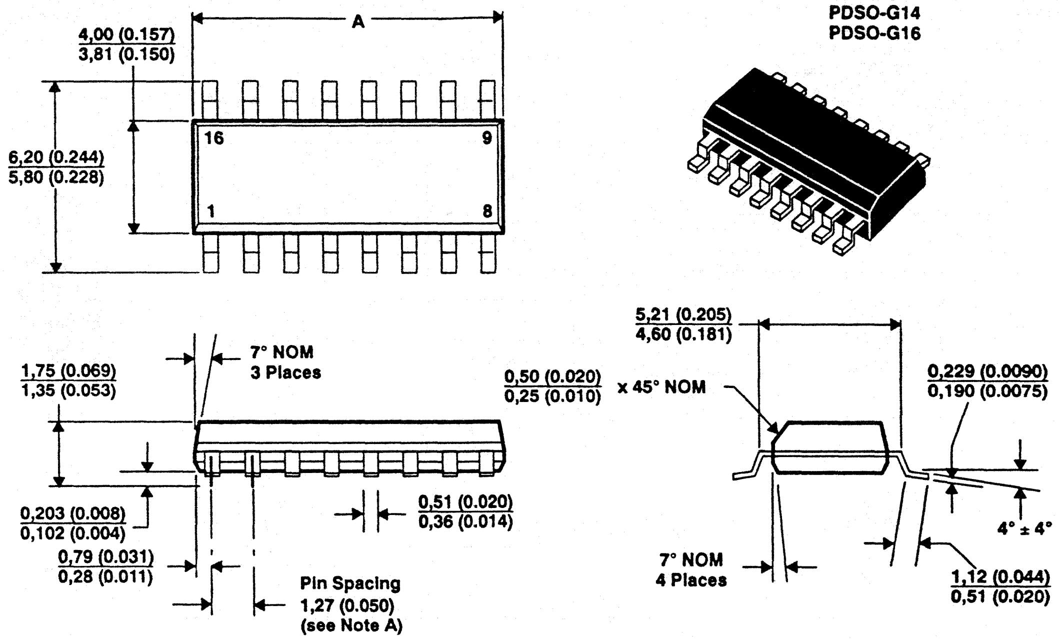
Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms

D008, D014, and D016
plastic small outline packages

Each of these small outline packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.

D008, D014, and D016
(16-pin package used for illustration)

Designation per JEDEC Std 30:
PDSO-G8
PDSO-G14
PDSO-G16



DIM \ PINS	8	14	16
A MIN	4,80 (0.189)	8,55 (0.337)	9,80 (0.386)
A MAX	5,00 (0.197)	8,74 (0.344)	10,00 (0.394)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,25 (0.010) radius of true position at maximum material condition.
B. Body dimensions do not include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 (0.006).
D. Lead tips to be planar within ±0,051 (0.002) exclusive of solder.

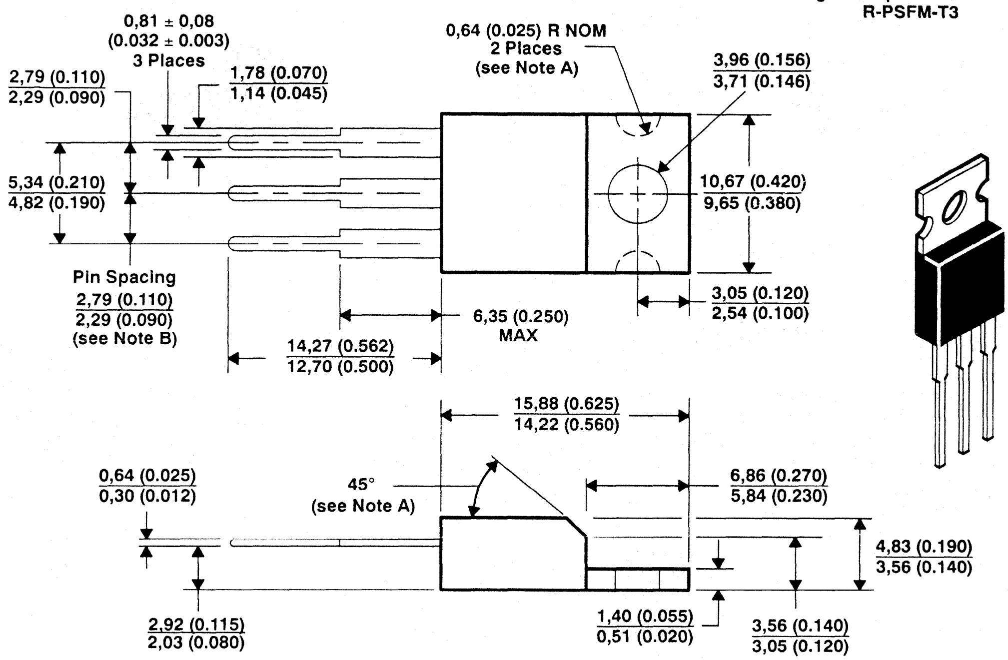
MECHANICAL DATA

KC003
plastic flange-mount package

This package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when the package is operated under high-humidity conditions.

KC003

Designation per JEDEC Std 30: R-PSFM-T3



The center terminal is in electrical contact with the mounting tab.
Falls within JEDEC TO-220AB dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Notches and/or mold chamfer may or may not be present.
B. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material conditions.

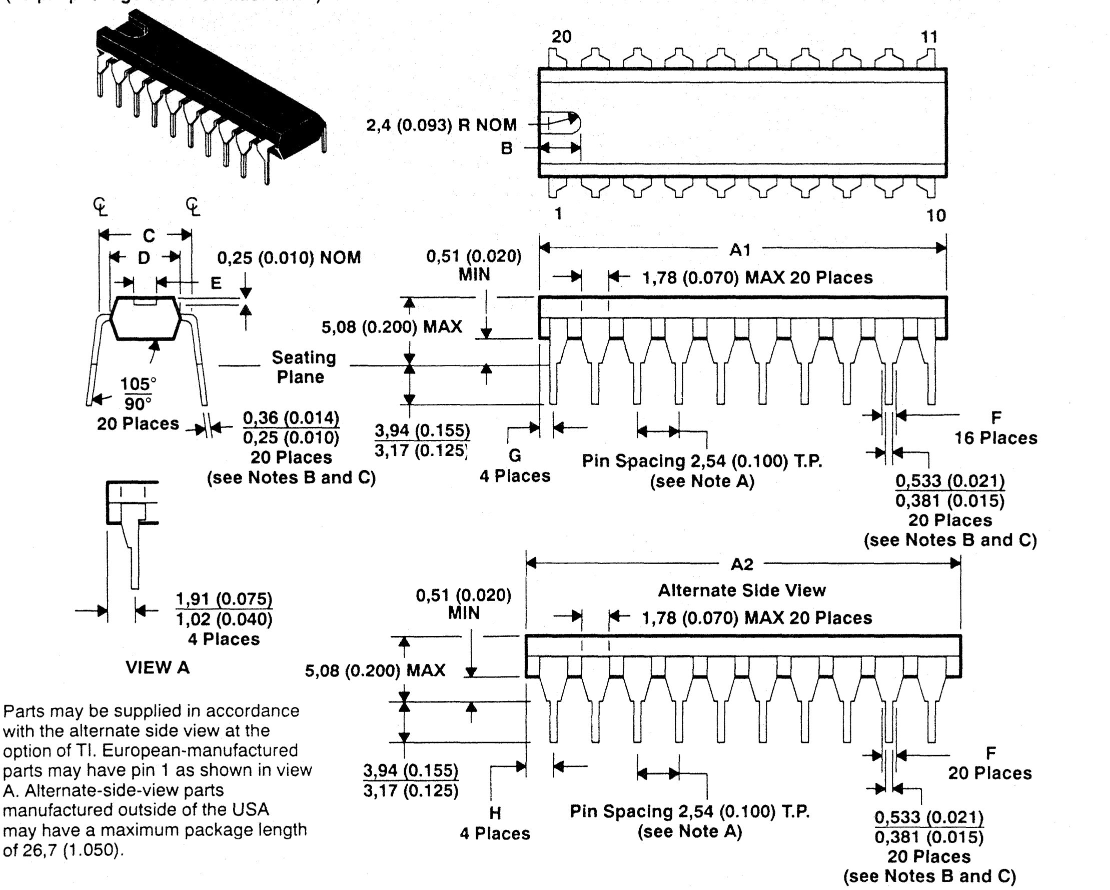
MECHANICAL DATA

N014, N016, N018, and N020
300-mil plastic dual-in-line package

These dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N014, N016, N018, AND N020
(20-pin package used for illustration)

Designation per JEDEC Std 30:
PDIP-T14



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

MECHANICAL DATA

N014, N016, N018, and N020
300-mil plastic dual-in-line package (continued)

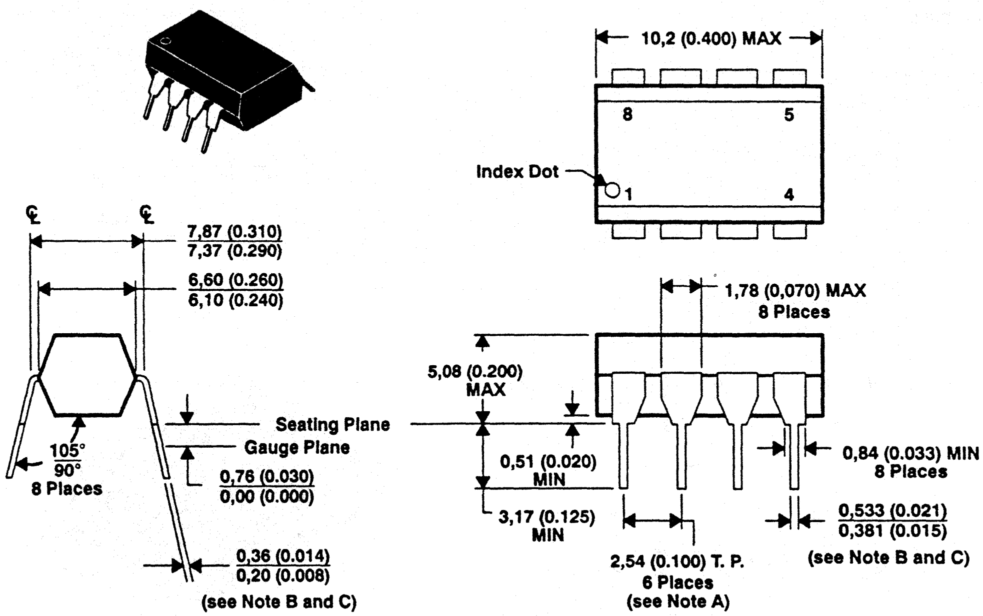
DIM \ PIN		14	16	18	20
A	MIN	18,0 (0.710)	(see Note A)	(see Note A)	23,22 (0.914)
	MAX	19,8 (0.780)	19,8 (0.780)	23,4 (0.920)	24,77 (0.975)
B	NOM	2,8 (0.110)	2,8 (0.110)	4,06 (0.160)	2,80 (0.110)
C	MIN	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)	7,37 (0.290)
	MAX	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)	7,87 (0.310)
D	MIN	6,10 (0.240)	6,10 (0.240)	(see Note A)	6,10 (0.240)
	MAX	6,60 (0.260)	6,60 (0.260)	6,99 (0.275)	7,11 (0.280)
E	NOM	2,0 (0.080)	2,0 (0.080)	2,03 (0.080)	2,0 (0.080)
F	MIN	0,84 (0.033)	0,84 (0.033)	0,89 (0.035)	0,84 (0.033)
G	MIN	(see Note B)	0,38 (0.015)	(See Note B)	1,68 (0.066)
	MAX	(see Note B)	1,65 (0.065)	(see Note B)	0,22 (0.009)
H	MIN	2,54 (0.100)	1,02 (0.040)	0,23 (0.009)	0,38 (0.015)
	MAX	1,52 (0.060)	2,41 (0.095)	1,91 (0.075)	1,27 (0.050)

NOTES: A. This packaging characteristic is not specified.
B. The 14-pin and 18-pin plastic dual-in-line package is only offered with the external pins shaped in their entirety.

P008
plastic dual-in-line package

This package consists of a circuit mounted on an 8-pin lead frame and encapsulated within a plastic compound.The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. The package is intended for insertion in mounting-hole rows on 7,62.(0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-plated lead require no additional cleaning or processing when used in soldered assembly.

P008



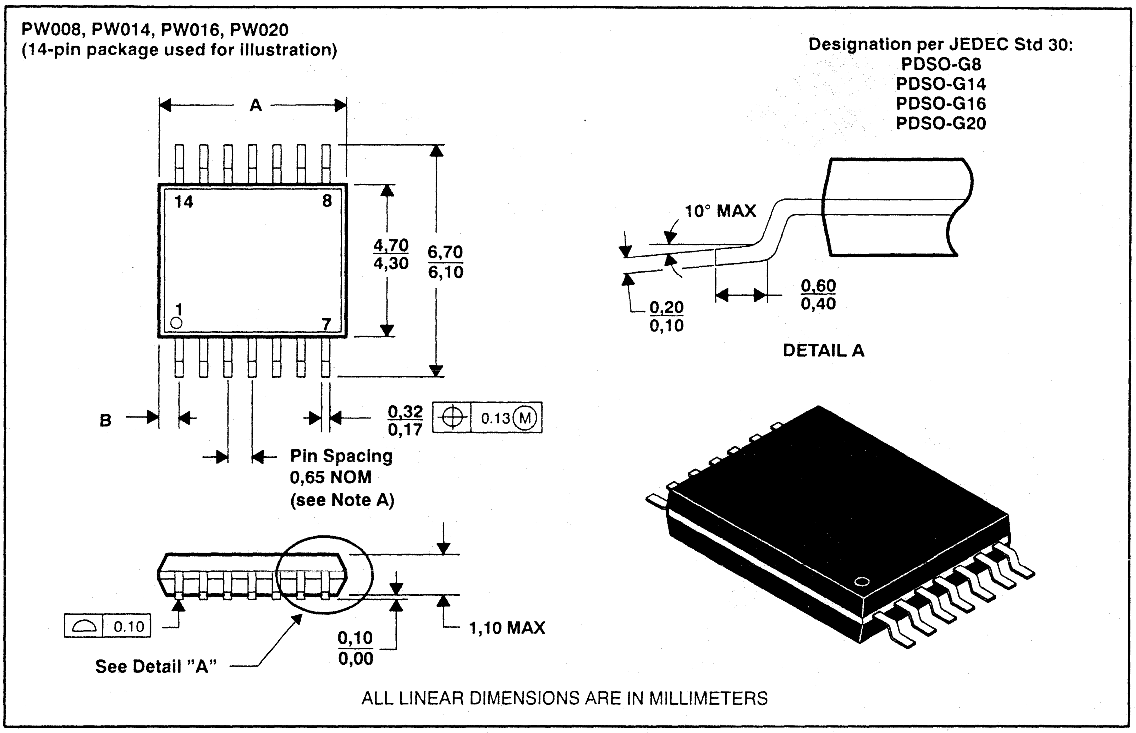
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN NINCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

MECHANICAL DATA

PW008, PW014, PW016, PW020
shrink small-outline packages

These shrunk small-outline packages consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high-humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Leads are within 0,25 mm radius of true position at maximum material condition.
B. Body dimensions include mold flash or protrusion.
C. Mold flash or protrusion shall not exceed 0,15 mm.
D. Lead tips to be planar within ±0,051 mm exclusive of solder.

PINS / DIM	8	14	16	20
A MIN	2,99	4,99	4,99	6,40
A MAX	3,03	5,30	5,30	6,80
B MAX	0,65	0,70	0,38	0,48

NOTES

NOTES

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